كلية الصفوة الجامعة

قسم هندسة تقنيات الحاسوب

محاضرات مادة الالكترونيك

المرحلة الثانية

1.Semiconductor

Semiconductors materials such as silicon (Si) and germanium (Ge), have electrical properties somewhere in the middle, between conductors and insulators. They are not good conductors nor good insulators, because their atoms are closely grouped together in a crystalline pattern called a “crystal lattice” but electrons are still able to flow, but only under special conditions.

The ability of semiconductors to conduct electricity can be greatly improved by replacing or adding certain donor or acceptor atoms to this crystalline structure thereby,

To producing more free electrons than holes adding a small percentage of another element to the base material (either silicon or germanium)

The most commonly used semiconductor basics material is **silicon**. Silicon has four valence electrons in its outermost shell which it shares with its neighboring silicon atoms to form full orbitals of eight electrons. The structure of the bond between the two silicon atoms is such that each atom shares one electron with its neighbor making the bond very stable.

As there are very few free electrons available to move around the silicon crystal, crystals of pure silicon or germanium are therefore good insulators, or at the very least very high value resistors.

Connecting a silicon crystal to a battery supply is not enough to extract an electric current from it. To do that we need to create a “positive” and a “negative” pole within the silicon allowing electrons to flow out of the silicon. These poles are created by doping the silicon with certain impurities.

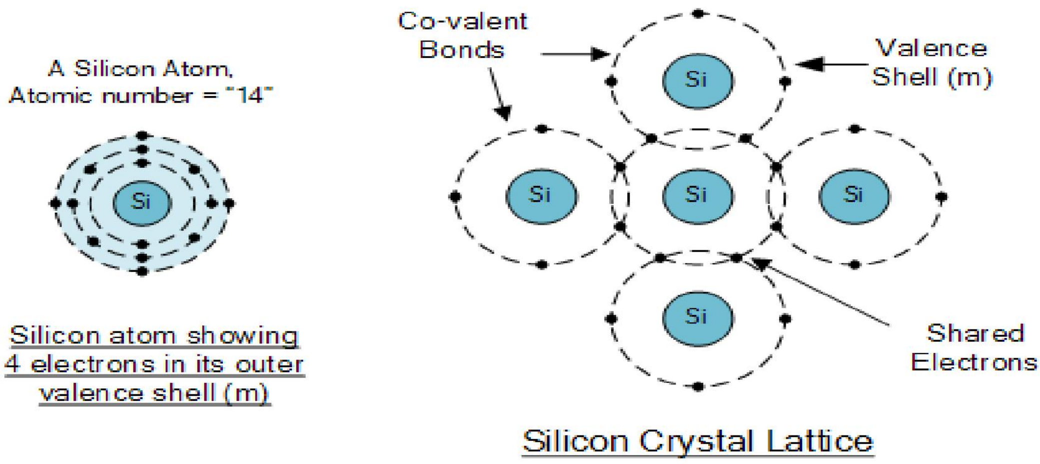


Figure.1: A Silicon Atom Structure

2. P-type

In a pure (intrinsic) Si or Ge semiconductor, each nucleus uses its four valence electrons to form four covalent bonds with its neighbors Each ionic core, consisting of the nucleus and non-valent electrons, has a net charge of +4, and is surrounded by 4 valence electrons. Since there are no excess electrons or holes in this case, the number of electrons and holes present at any given time will always be equal.

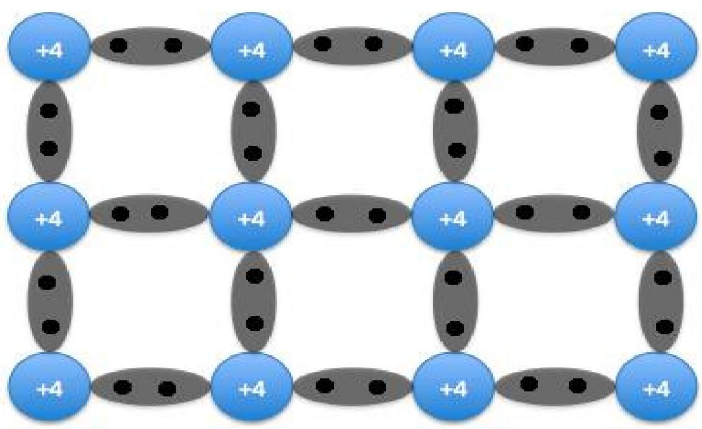


Figure.2: An intrinsic semiconductor.

if one of the atoms in the semiconductor lattice is replaced by an element with three valence electrons, such as a Group 3 element like Boron (B) or Gallium (Ga), the electron-hole balance will be changed. This impurity will only be able to contribute three valence electrons to the lattice, therefore leaving one excess hole (figure.3). Since holes will "accept" free electrons, a Group 3 impurity is also called an acceptor.

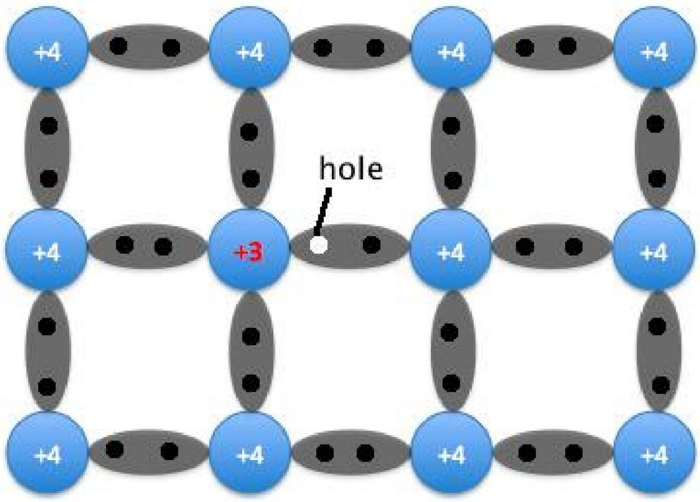


Figure .3: A semiconductor doped with an acceptor

Because an acceptor donates excess holes, which are positively charged, a semiconductor that has been doped with an acceptor is called a p-type semiconductor; "p" stands for positive. Notice that the material remains electrically neutral. In a p-type semiconductor, current is largely carried by the holes, which outnumber the free electrons. In this case, the holes are the majority carriers, while the electrons are the minority carriers.

3. N-type

We can also replace an atom with five valence electrons, such as the Group 5 atoms arsenic (As) or phosphorus (P). In this case, the impurity adds five valence electrons to the lattice where it can only hold four. This means that there is now one excess electron in the lattice (Figure.4). Because it donates an electron, a Group 5 impurity is called a donor. Note that the material remains electrically neutral.

Donor impurities donate negatively charged electrons to the lattice, so a semiconductor that has been doped with a donor is called an n-type semiconductor; "n" stands for negative. Free electrons outnumber holes in an n-type material, so the electrons are the majority carriers and holes are the minority carriers.

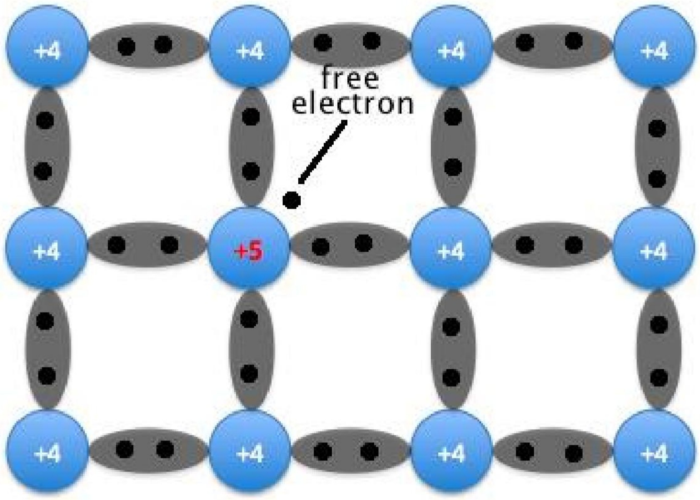
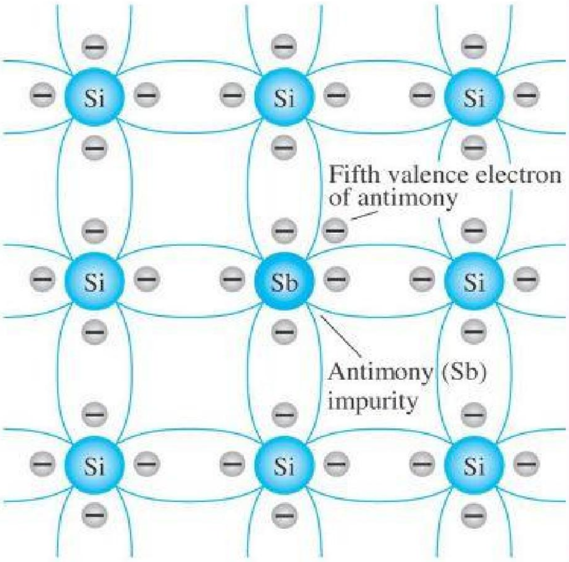


Figure.4: A semiconductor doped with a donor

n-Type and p-Type materials

n-Type Material

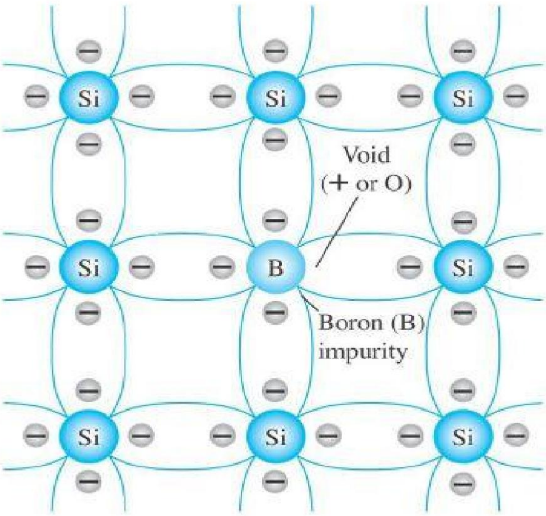


Doping with Sb, (antimony)

- n-Type materials are created by adding elements with **five** valence electrons such as antimony, arsenic, and phosphorous.
- There is a fifth electron due to the (Sb) atom that is relatively free to move in the n-Type material.
- The atoms (in this case is antimony (Sb)) are called **donor atoms.**

n-Type and p-Type materials

p-Type Material



Boron (B)

- p-Type materials are created by adding atoms with **three** valence electrons such as boron, gallium, and indium.
- In this case, an insufficient number of electrons to complete the covalent bonds.
- The resulting vacancy is called a "**hole**" represented by small circle or plus sign indicating absence of a negative charge.
- The atoms (in this case boron(B)) are called **acceptor atoms**.

4. PN Junction

A PN-junction is formed when an N-type material is fused together with a P-type material creating a semiconductor diode (Figure.5)

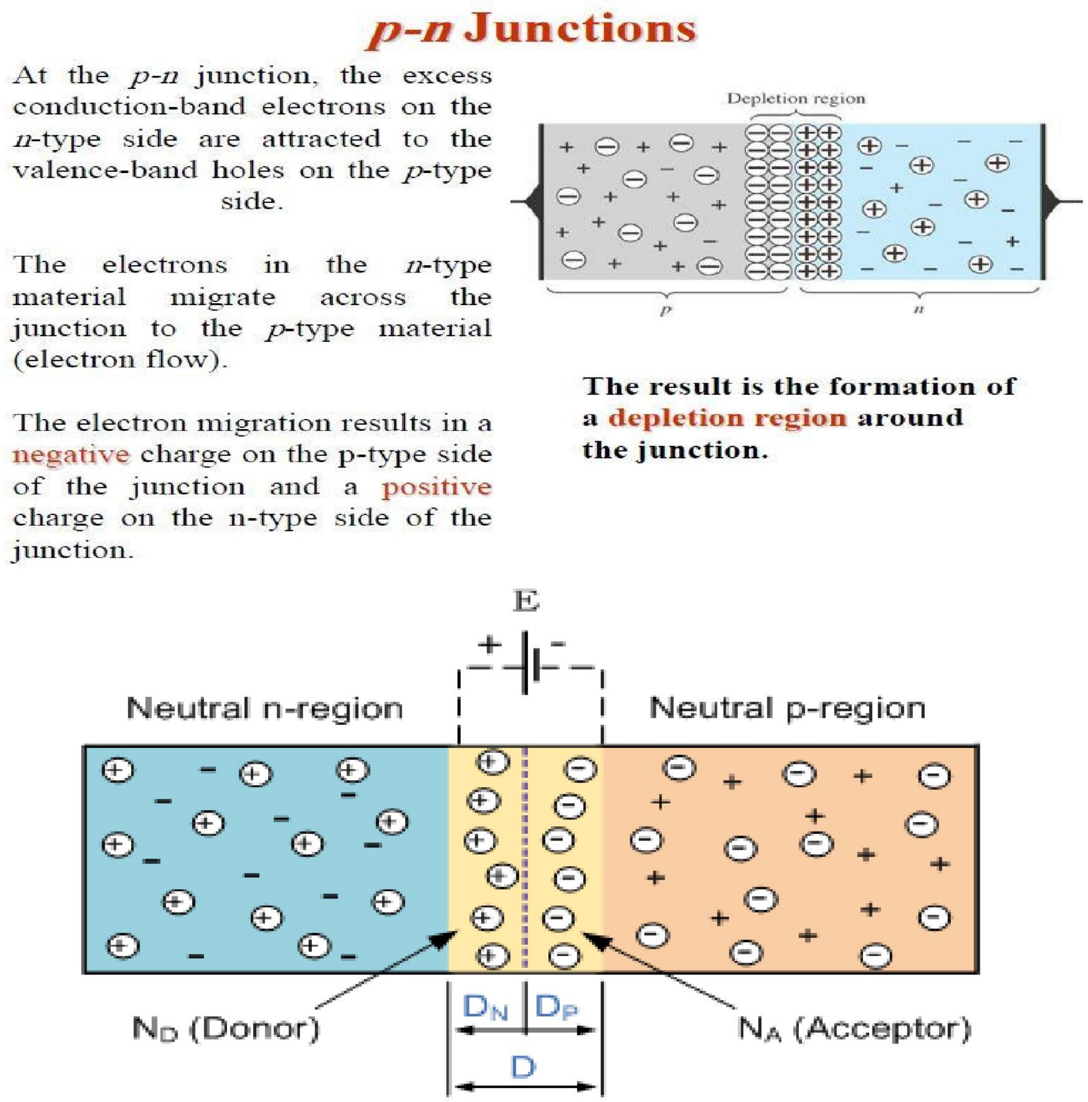


Figure.5: p-n junction structure

6. Semiconductor Diode

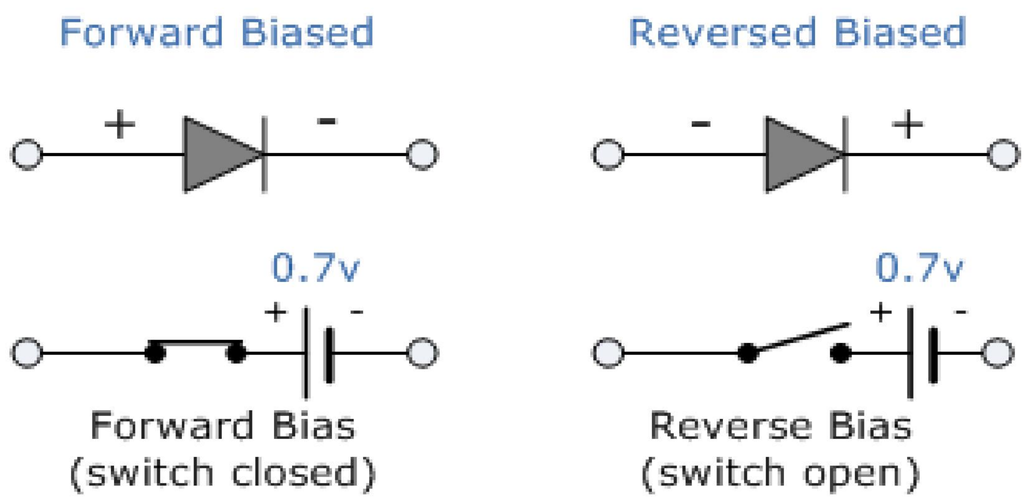
the n- and p-type materials were introduced. The semiconductor diode is formed by simply bringing these materials together (constructed from the same base—Ge or Si) the two materials are “joined” the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction.

This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region

7. Biasing of A Diode

the diode is a two-terminal device the application of a voltage across its terminals leaves three possibilities: no bias **(VD = 0V)**, forward bias **(VD >V),** and reverse bias **(VD < V).** Each is a condition that will result in a response that the user must clearly understand if the device is to be applied effectively.

For silicon diode the minimum voltage to operate the diode is 0.7 v
For germanium diode the minimum voltage to operate the diode is 0.3 v

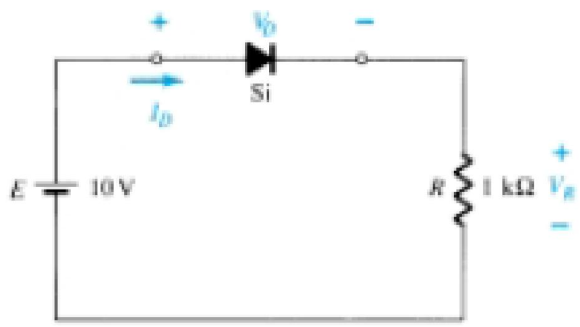


EXAMPLE 1

For the series diode configuration bellow determine the following

(a) V_D and I_D

(b) V_R



Solution:

since the diode is Si then

$V_D = 0.7$ V

Appling KVL

$E - V_D - V_R = 0$

$10 - 0.7 = V_R$

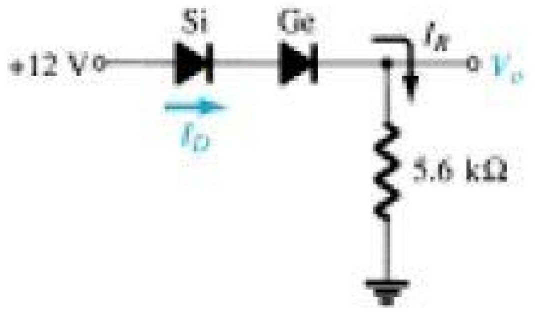
$V_R = 9.3$ V

V = I.R (ohm's law)

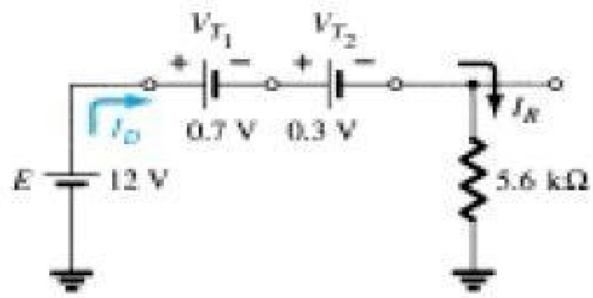
$I_R = \frac{VR}{R} = \frac{9.3\ V}{1\ K\Omega} = 9.3$ mA which is the same value of I_D

EXAMPLE 2

Determine V_R and I_D for the series circuit of Figure bellow



Solution:

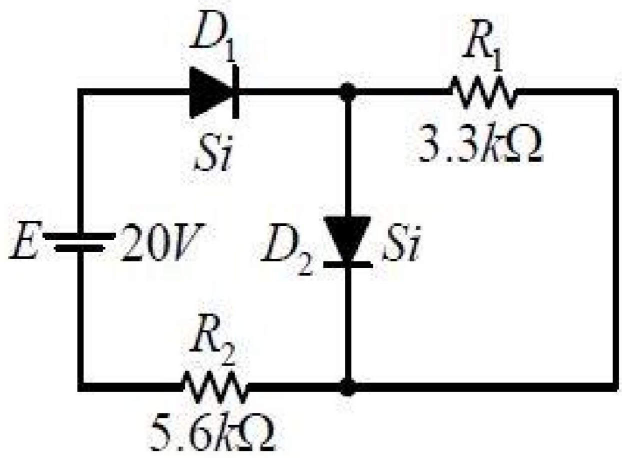


$VR = E - V_{T1} - V_{T2} = 12\ V - 0.7\ V - 0.3\ V = 11\ V$

$I_D = I_R = \frac{VR}{R} = \frac{11\ V}{5.6\ K\Omega} = 1.96\ mA$.

EXAMPLE 3

Determine the currents I_{D1} , I_{D2} and I_{R1} for this circuit



Solution:

$$I_{R_1} = \frac{V_{D_2}}{R_1} = \frac{0.7}{3.3k} = 0.212mA.$$

Appling KVL yields:

$$-V_{R_2} + E - V_{D_1} - V_{D_2} = 0$$

and $\quad V_{R_2} = E - V_{D_1} - V_{D_2} = 20 - 0.7 - 0.7 = 18.6V$,

with $\quad I_{D_1} = \dfrac{V_{R_2}}{R_2} = \dfrac{18.6}{5.6k} = 3.32mA.$

Finally, $I_{D_2} = I_{D_1} - I_{R_1} = 3.32m - 0.212m = 3.108mA$.

8. Half-Wave Rectification

A rectifier is a circuit which converts the Alternating Current (AC) input power into a Direct Current (DC) output power. The simplest half wave rectifier circuit with a time-varying signal appears in Figure.6 For the moment we will use the ideal model (note the absence of the Si or Ge label to denote ideal diode) to ensure that the approach is not clouded by additional mathematical complexity.

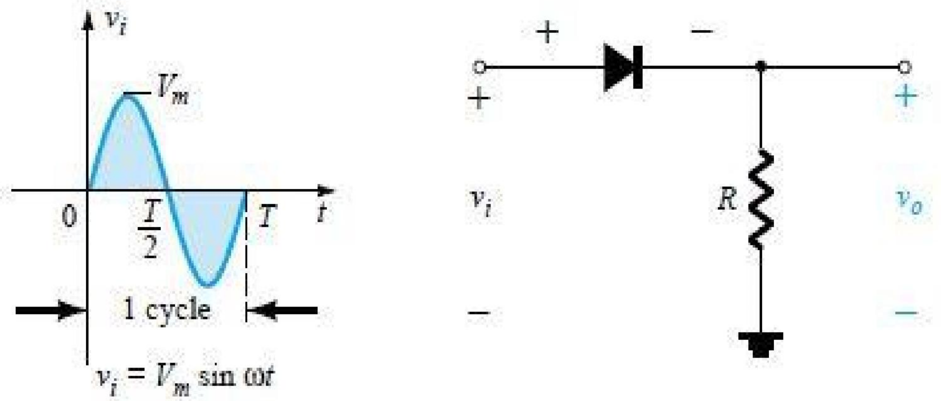


Figure.6: Sinusoidal Inputs; Half-Wave Rectification

the following formula is used to determine the V_{dc} for the ideal diode

$$\boxed{V_{dc} = 0.318 V_m} \quad \text{half-wave}$$

While the following formula is used to determine the V_{dc} for the Si or Ge diode

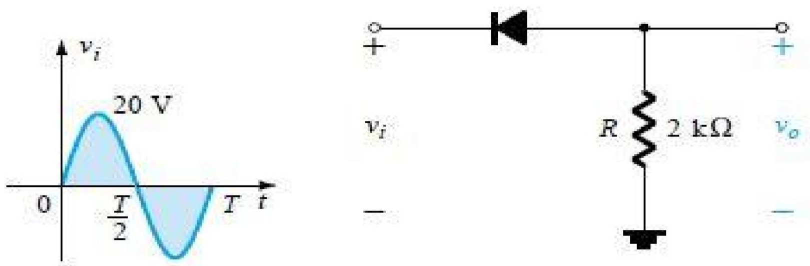
$$\boxed{V_{dc} \cong 0.318(V_m - V_T)}$$

EXAMPLE 4

(a) Sketch the output vo and determine the dc level of the output for the network bellow

(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.

(c) Repeat parts (a) and (b) if Vm is increased to 200 V and compare solutions

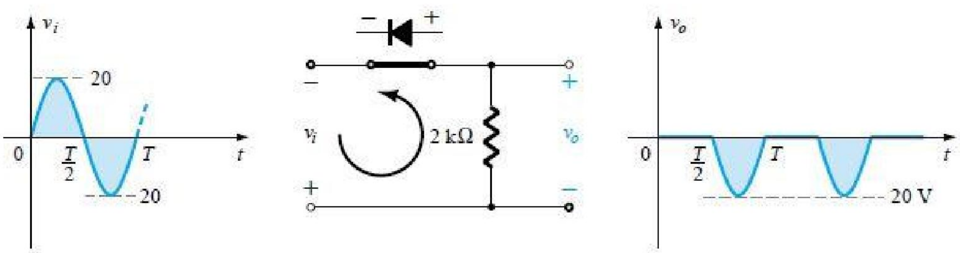


Solution:

(a) In this situation the diode will conduct during the negative part of the input as
shown in Figure and vo will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = -6.36\text{ V}$$

The negative sign indicates that the polarity of the output is opposite to the defined in this figure



(b) Using a silicon diode, the output will be

$V_{dc} = -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) = -6.14\text{ V}$

(c) ???

9. Full-Wave Rectification

A Full wave rectifier is a circuit arrangement which makes use of both half cycles of input alternating current (AC) and converts them to direct current (DC). In our tutorial on Half wave rectifiers, we have seen that a half wave rectifier makes use of only one-half cycle of the input alternating current. Thus, a full wave rectifier is much more efficient than a half wave rectifier. This process of converting both half cycles of the input supply (alternating current) to direct current (DC) is termed full wave rectification.

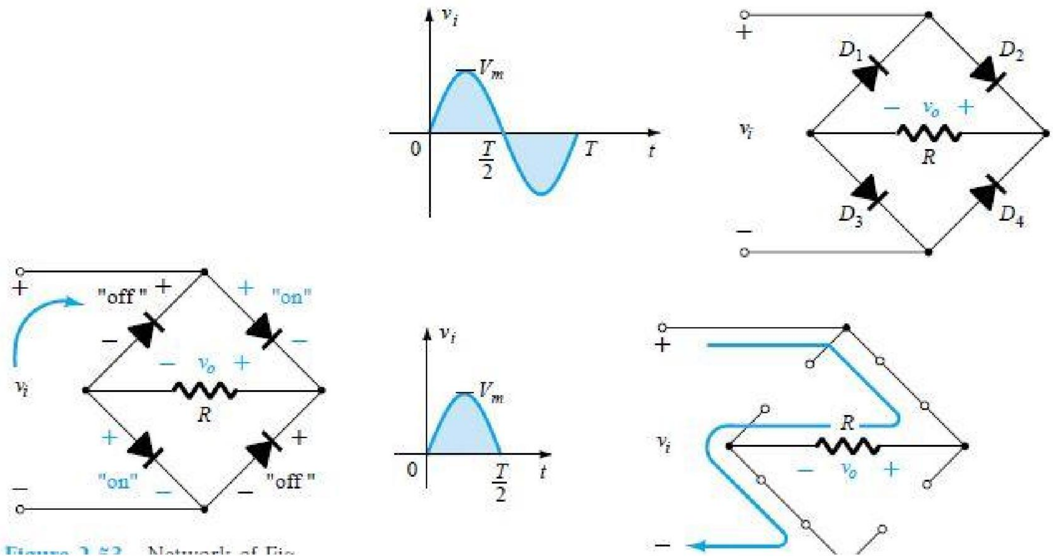


Figure.7: A Full wave rectifier

the dc level is now twice that obtained for a half-wave system and the value will be doubled

$$Vdc = 2(0.318Vm)$$

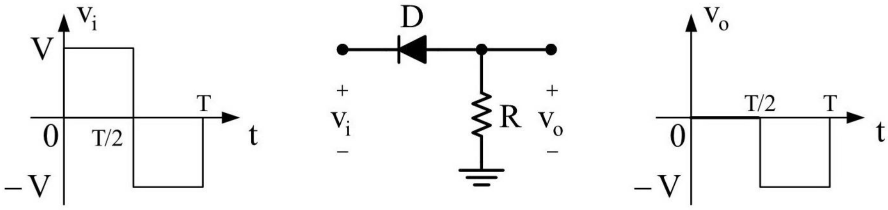
$$\boxed{V_{dc} = 0.636V_m} \quad \text{full-wave}$$

Diode Clipping Circuits

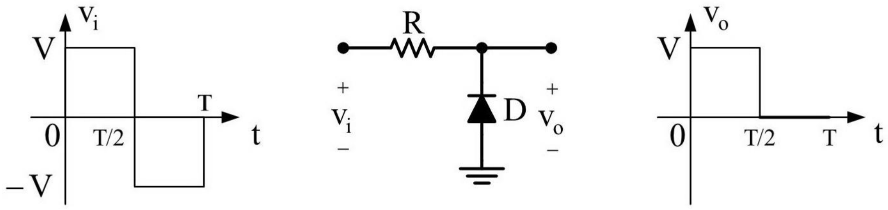
Basic Definition:

There are a variety of diode circuits called **clippers** (**limiters** or **selectors**) that have the ability to "clip" off a portion of the input signal above (**positive**) or below (**negative**) certain level without distorting the remaining part of the alternating waveform. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: **series** and **parallel**. The series configuration is dined as one where the diode is in series with the load. While the parallel variety has the diode in a branch parallel to the load (see Fig. 3-1).



Simple Series (Positive) Clipper



Simple Parallel (Negative) Clipper

Fig. 3-1

Example 3-1:

Biased Series (Negative) Clipper, see Fig. 3-2.

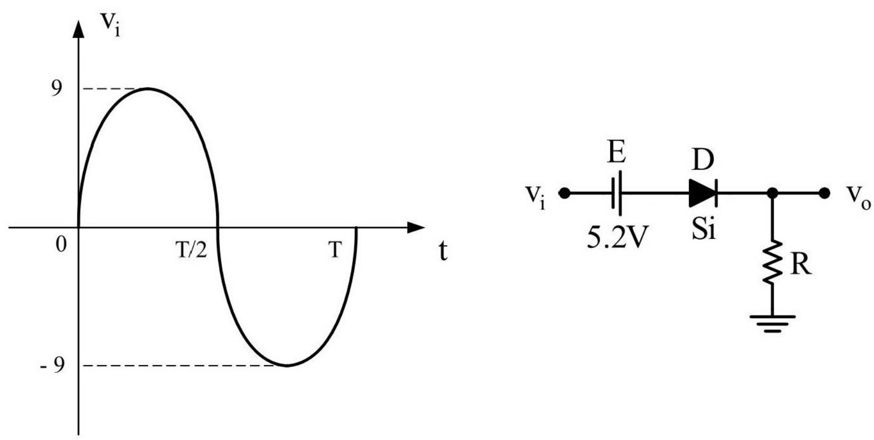
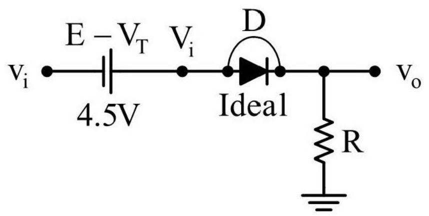
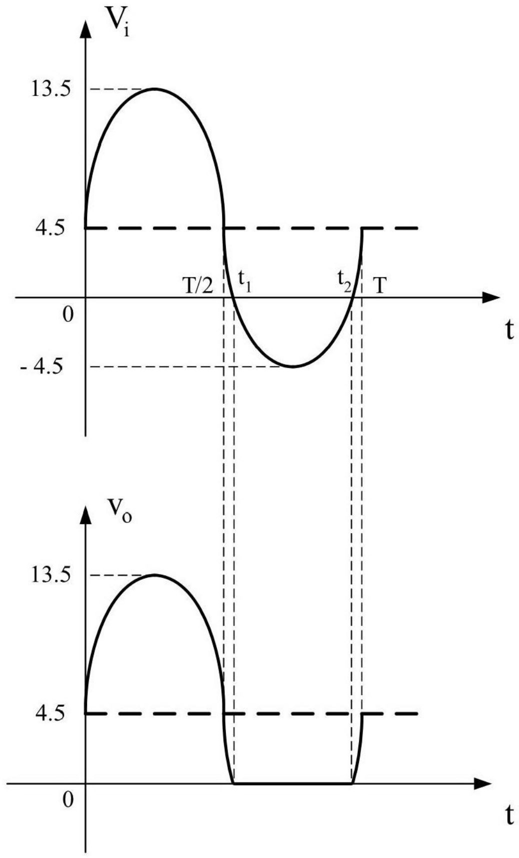


Fig. 3-2



For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow T$; D ON, and $v_o = v_i + 4.5$ V.
For $t = t_1 \rightarrow t_2$; D OFF, and $v_o = 0$ V.



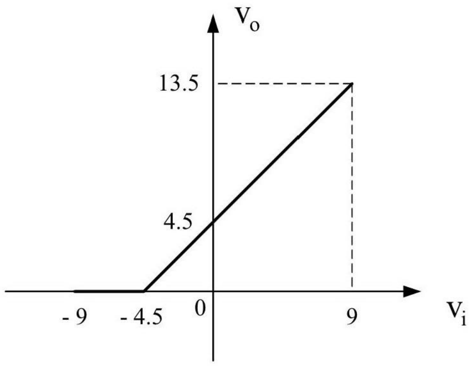


Fig. 3-2 (cont.)

Example 3-2:

Biased Parallel (Positive) Clipper, see Fig. 3-3.

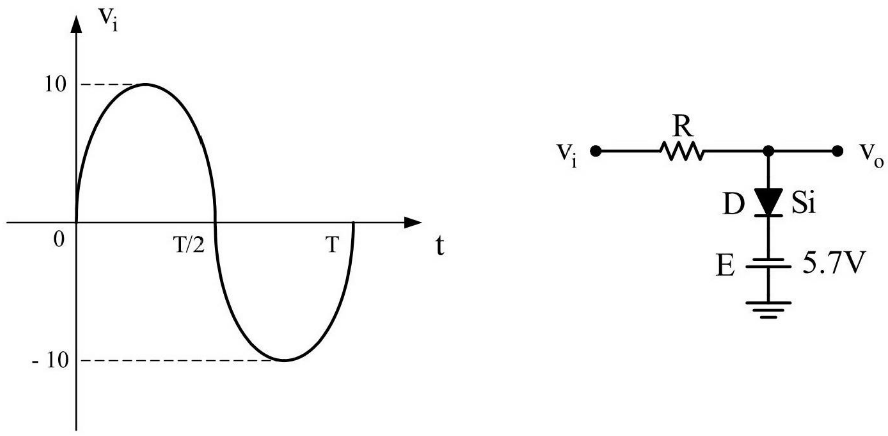
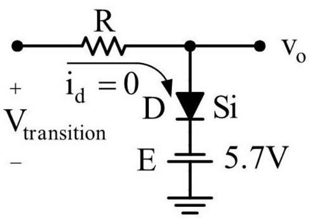
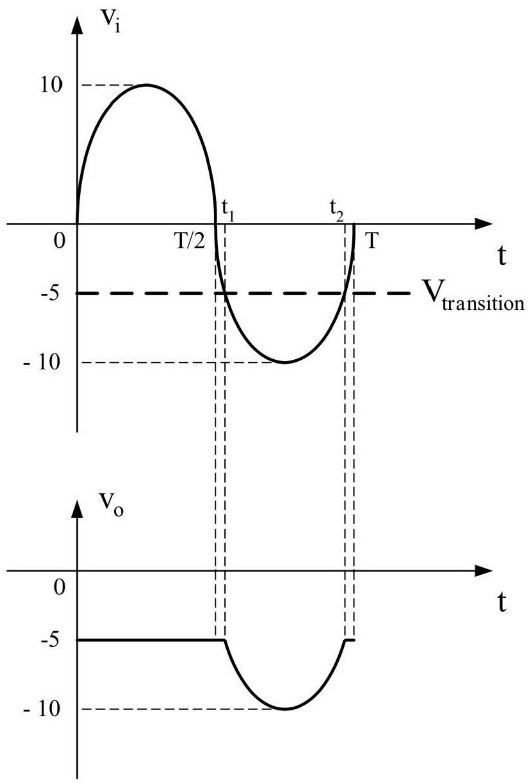


Fig. 3-3



$V_{transition} - i_d R - V_d + E = 0;$
$V_{transition} = 0.7 - 5.7 = -5$ V.
For $t = 0 \rightarrow t_1$ and $t_2 \rightarrow T$; D ON,
and $v_o = -5$ V.
For $t = t_1 \rightarrow t_2$; D OFF,
and $v_o = v_i$.



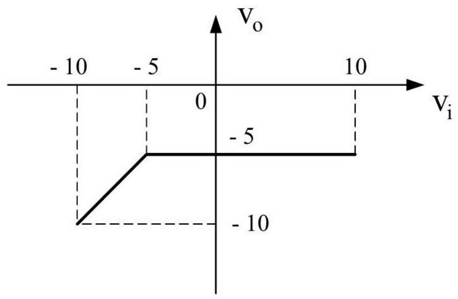


Fig. 3-3 (cont.)

Summary:

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 3-4.

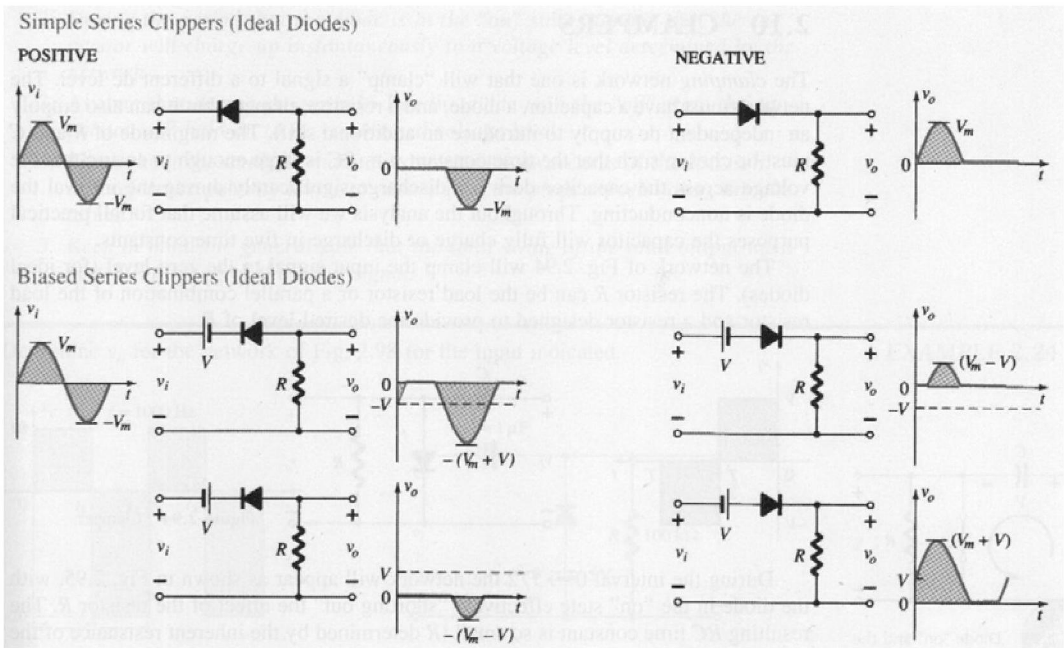


Fig. 3-4

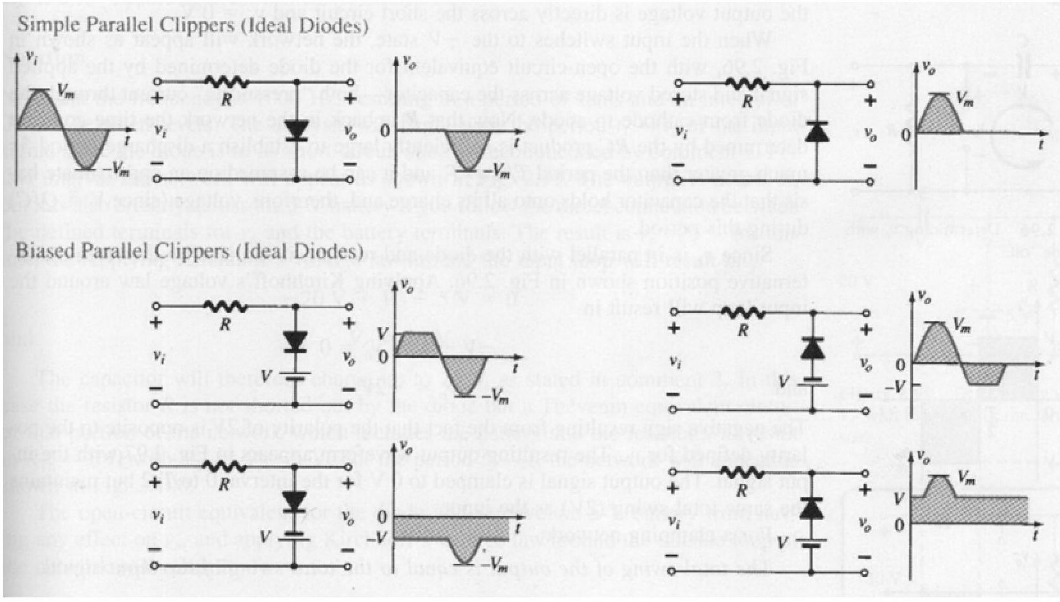


Fig. 3-4 (cont.)

Example 3-3:

Double Diode Series Clipper, see Fig. 3-5.

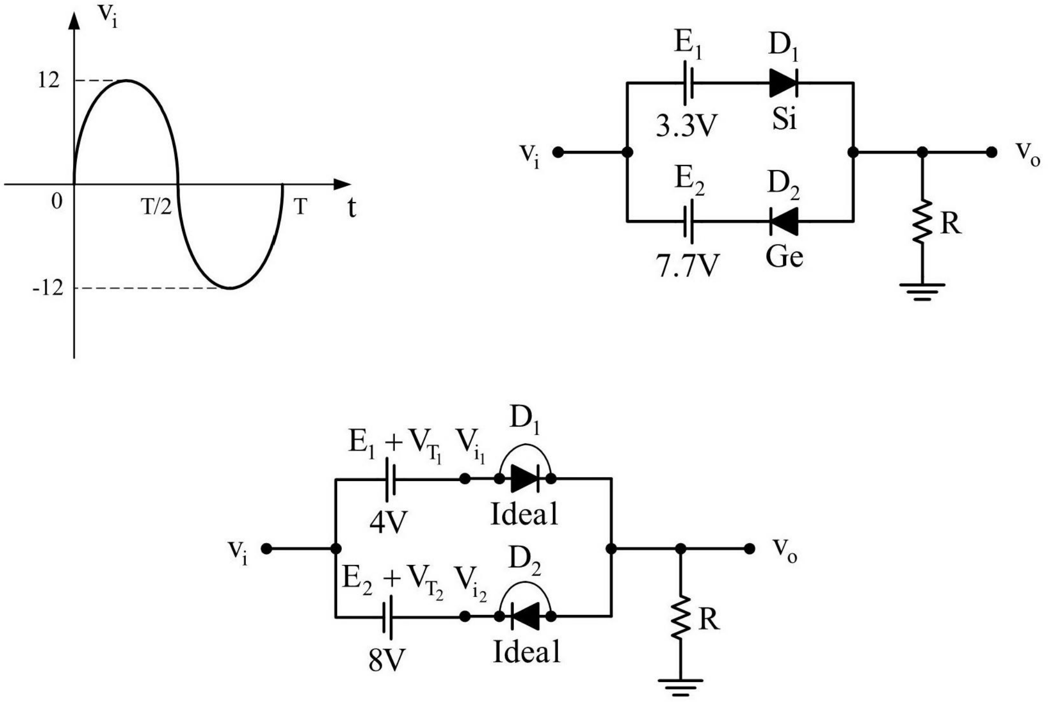
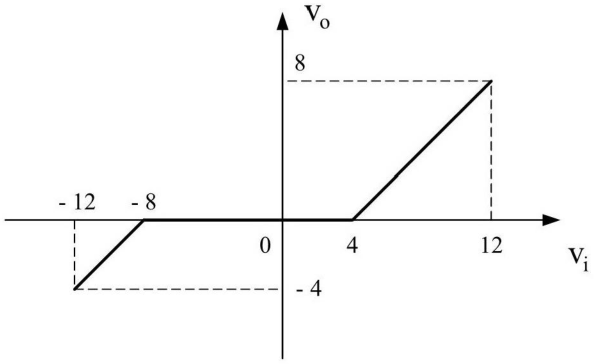


Fig. 3-5

For $t = 0 \rightarrow t_1$, $t_2 \rightarrow t_3$, and $t_4 \rightarrow T$; both D_1 and D_2 will be OFF, and $v_o = 0$ V.

For $t = t_1 \rightarrow t_2$; D_1 ON while D_2 OFF, and $v_o = V_{i_1} = v_i - 4$ V.

For $t = t_3 \rightarrow t_4$; D_1 OFF while D_2 ON, and $v_o = V_{i_2} = v_i + 8$ V.



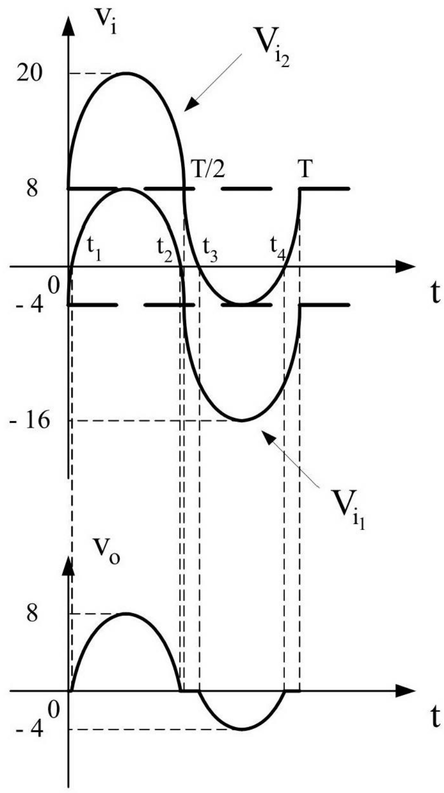
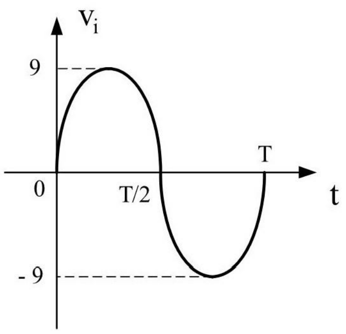
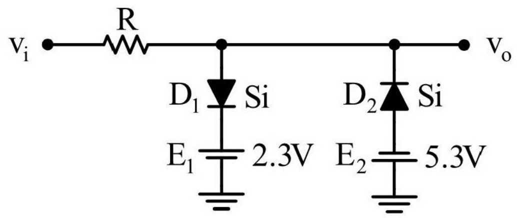


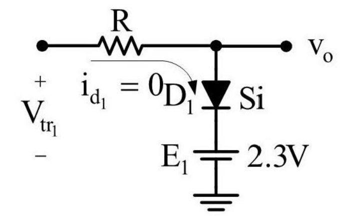
Fig. 3-5 (cont.)

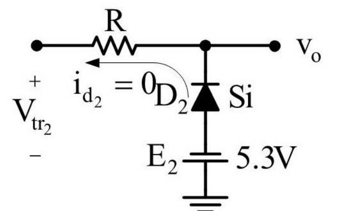
Example 3-4:

Double Diode Parallel Clipper, see Fig. 3-6.









$V_{tr_1} - i_{d_1} R - V_d - E_1 = 0;$

$V_{tr_1} = 0.7 + 2.3 = 3$ V.

$V_{tr_2} + i_{d_2} R + V_d + E_2 = 0;$

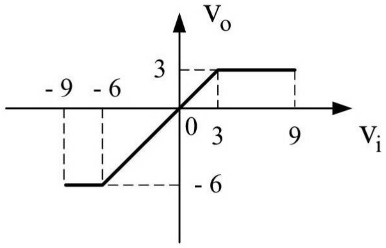
$V_{tr_2} = -0.7 - 5.3 = -6$ V.

Fig. 3-6

For $t = 0 \rightarrow t_1$, $t_2 \rightarrow t_3$, and $t_4 \rightarrow T$; both D_1 and D_2 will be OFF, and $v_o = v_i$.

For $t = t_1 \rightarrow t_2$; D_1 ON while D_2 OFF, and $v_o = 3$ V.

For $t = t_3 \rightarrow t_4$; D_1 OFF while D_2 ON, and $v_o = -6$ V.



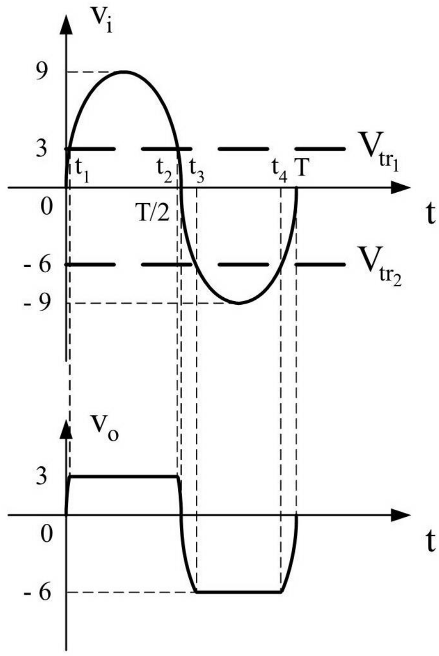


Fig. 3-6 (cont.)

Diode Clamping Circuits

Basic Definition:

The clamping circuit (**clamper**) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval $(T/2)$ the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$\boxed{5\tau = 5RC >> \frac{T}{2} = \frac{1}{2f}} \qquad [4.1]$$

Example 4-1:

Determine the output (v_o) for the circuit of Fig. 4-1 for the input (v_i) shown.

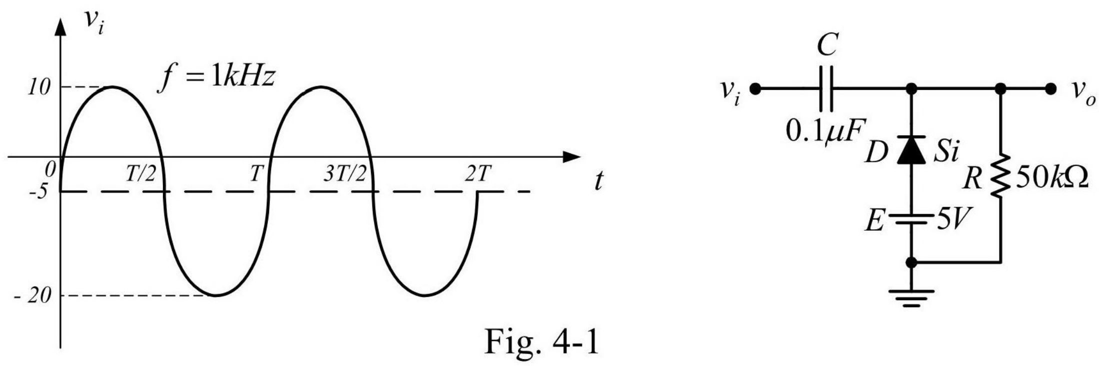


Fig. 4-1

Solution:

The analysis of clamping circuits are started by considering that the part of the input signal that will forward bias the diode. For the circuit of Fig. 4-1, the diode is forward bias ("on" state) during the negative half period of the input signal (v_i) and the capacitor will charge up instantaneously to a voltage level determined by the circuit of Fig. 4-2.

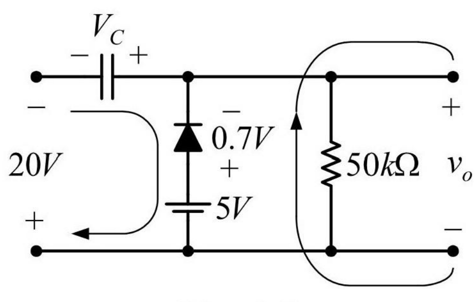


Fig. 4-2

For the input section KVL will result in

$$- 20 + V_C + 0.7 - 5 = 0 \quad => \quad V_C = 24.3 \text{ V}.$$

The output voltage (v_o) can be determined by KVL in the output section

$$+ 5 - 0.7 - v_o = 0 \quad => \quad v_o = 4.3 \text{ V}.$$

Now check that the capacitor will hold on or not its establish voltage level during the period (positive half period in case of Example 4-1) when the diode is in the "off" state (reverse bias). The total time constant 5τ of the discharging circuit of Fig. 4-3 is determined by the product $5RC$ and has the magnitude

$$5\tau = 5RC = 5\ (50\times10^3)\ (0.1\times10^{-6}) = 25 \text{ ms}.$$

The frequency (f) is 1 kHz, resulting in a period of 1 ms and an interval of 0.5 ms between levels, that is

$$T/2 = 1/(\ 2f\ ) = 1/(2 \times 1\times10^3) = 0.5 \text{ ms}.$$

We find that

$$5\ \tau >> T/2 \quad (\ 25\text{ms} / 0.5\text{ms} = 50 \text{ times}).$$

So that, it is certainly a good approximation that the capacitor will hold its voltage (24.3 V) during the discharge period between pulses of the input signal.

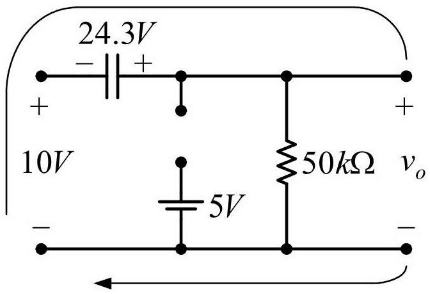


Fig. 4-3

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying KVL around the outside loop of circuit will result in

$$+ 10 + 24.3 - v_o = 0 \quad => \quad v_o = 34.3 \text{ V}.$$

The resulting output appears in Fig. 4-4, where the input and the output swing are the same.

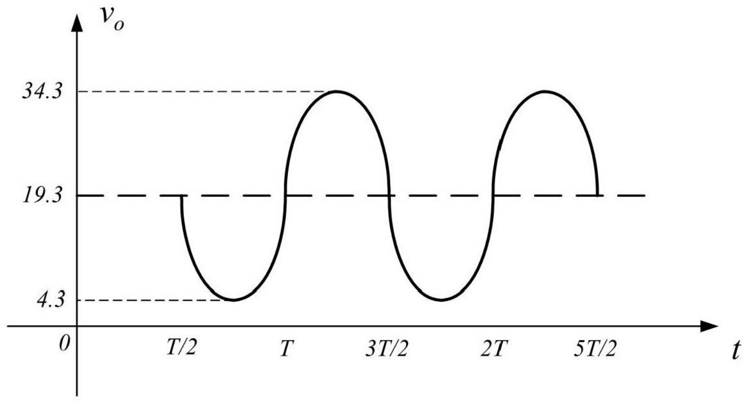


Fig. 4-4

Example 4-2:

Using silicon diode, design a clamper circuit that will produce output $v_o = 10Sin\omega t - 5$ V when the input is $v_i = 10Sin\omega t + 5$ V. Draw the circuit diagram and the input and output signals.

Solution:

From the input (v_i) and output (v_o) signals, we have a negative biased clamper. Therefore, the diode is forward bias ("on" state) during the positive half period of the input signal (v_i). The output voltage (v_o) at this positive period can be determined by KVL in the output section of the circuit shown in Fig. 4-5.

$$E + 0.7 - v_o = 0 \quad => \quad E = 5 - 0.7 = 4.3 \text{ V}.$$

For the input section KVL will result in

$$15 - V_C - 5 = 0 \quad => \quad V_C = 10 \text{ V}.$$

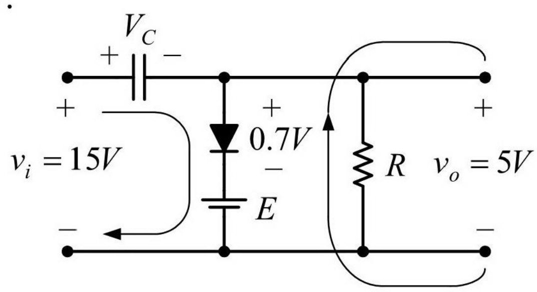


Fig. 4-5

The circuit diagram and the input and output signals are shown in Fig. 4-6.

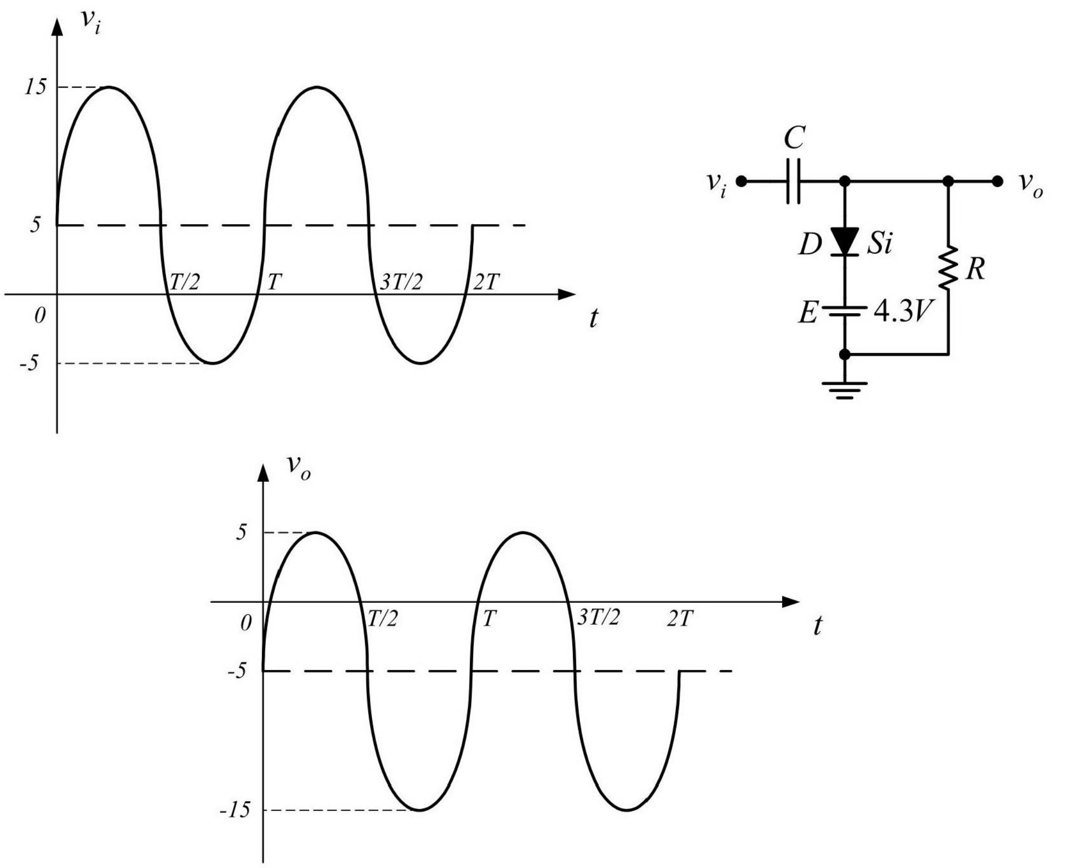
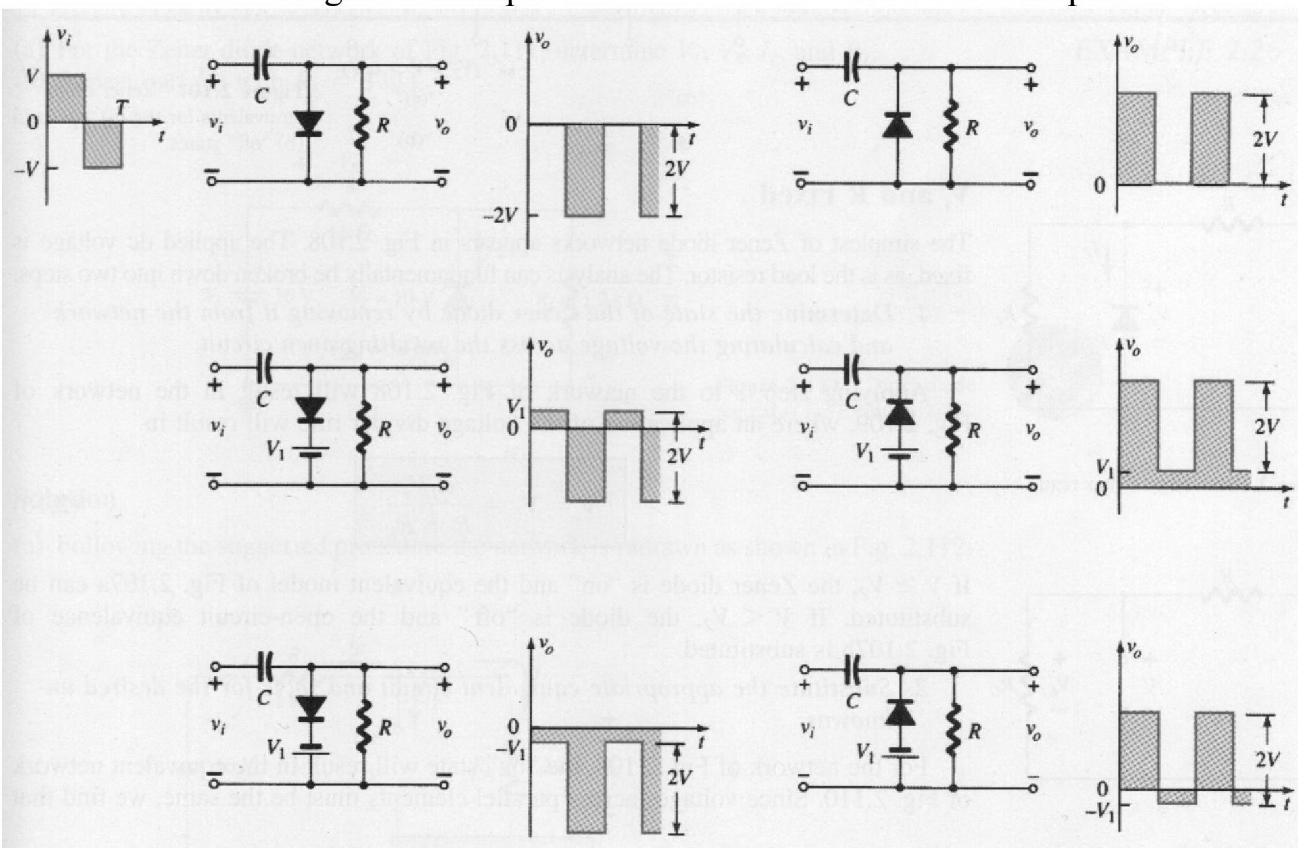


Fig. 4-6

Summary:

A number of clamping circuits and their effect on the square-wave input signal are shown in Fig. 4-7.

Negative Clampers Positive Clampers



Clampers with ideal diodes and $5\tau = 5RC >> T/2$

Fig. 4-7

ELECTRONIC DEVICES

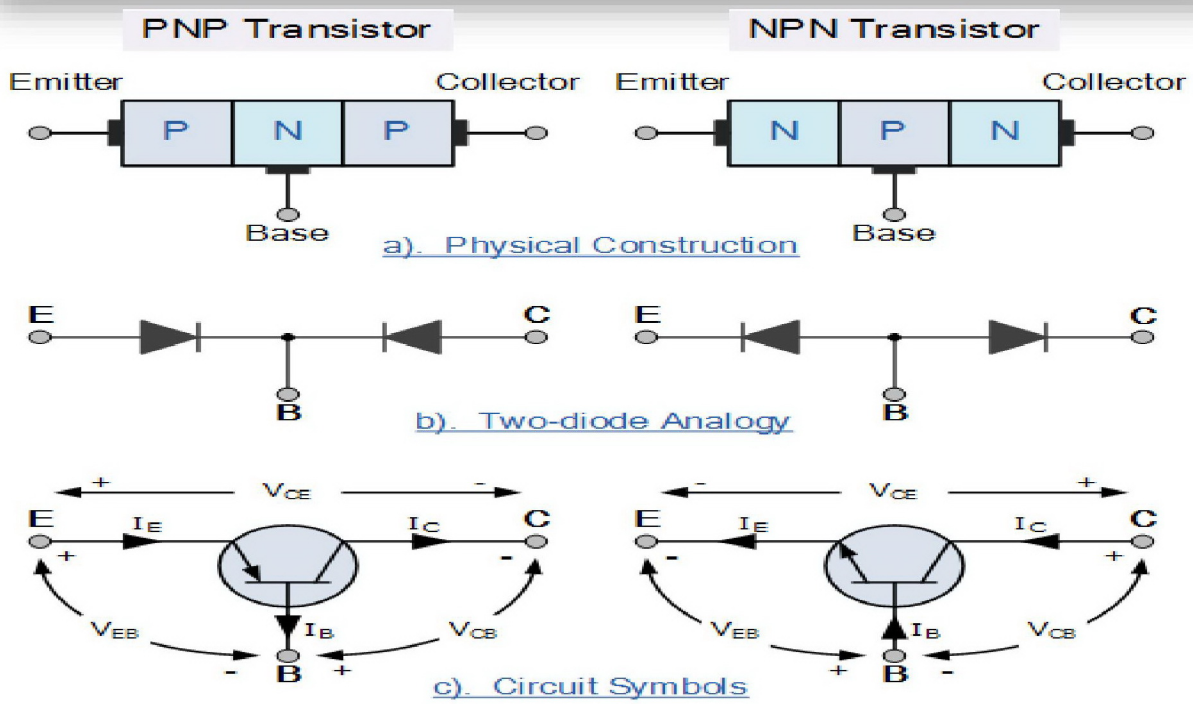
Contents

Electronic Devices

3 Bipolar Junction Transistors

Transistor Construction

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor,* while the latter is called a *pnp transistor.* Both are shown in Fig.



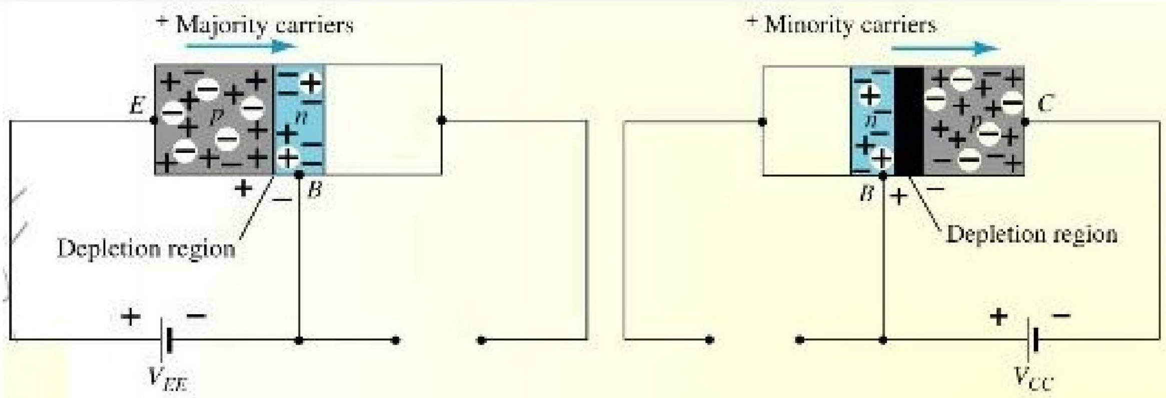
For the biasing shown in Fig. the terminals have been indicated by the capital letters *E* for *emitter*, *C* for *collector*, and *B* for *base*.

TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor of Fig. . The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged.

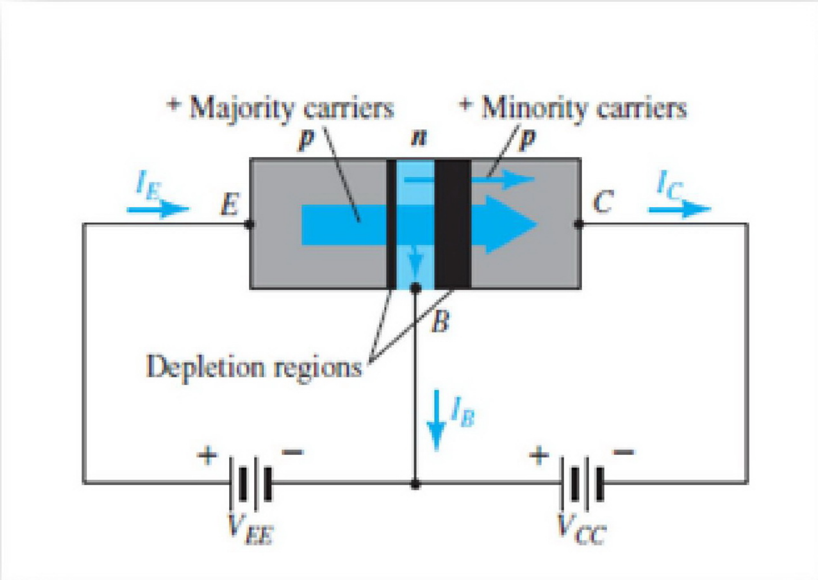
Note the similarities between this situation and that of the *forward-biased* diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

Consider the similarities between this situation and that of the *reverse-biased* diode . Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow,



Forward-biased junction of a pnp transistor

Reverse-biased junction of a pnp transistor

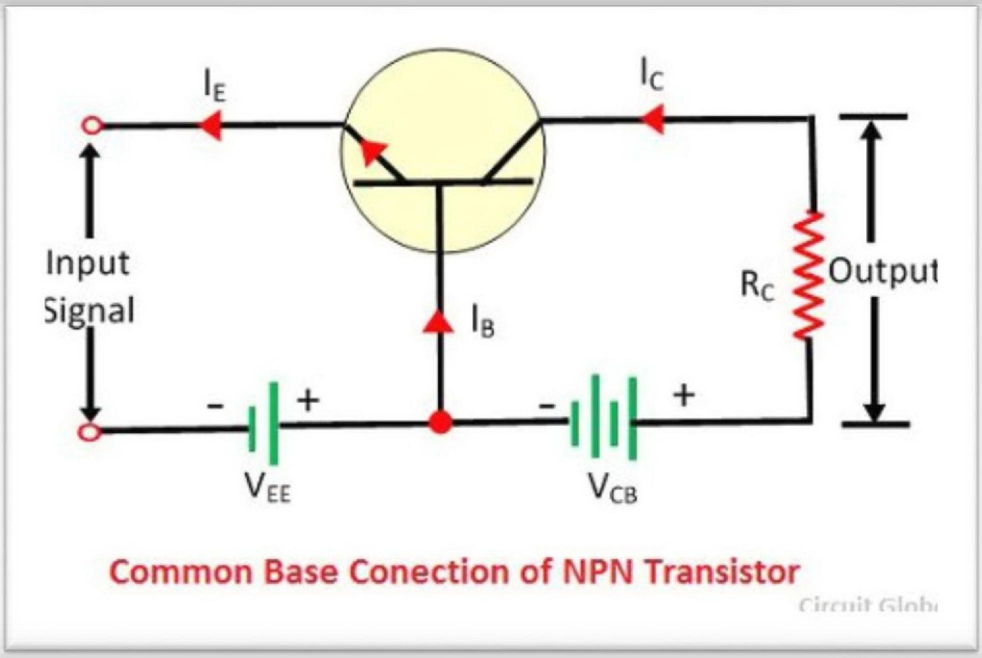


Applying Kirchhoff's current law to the transistor of Fig. above we obtain

$$\boxed{I_E = I_C + I_B}$$

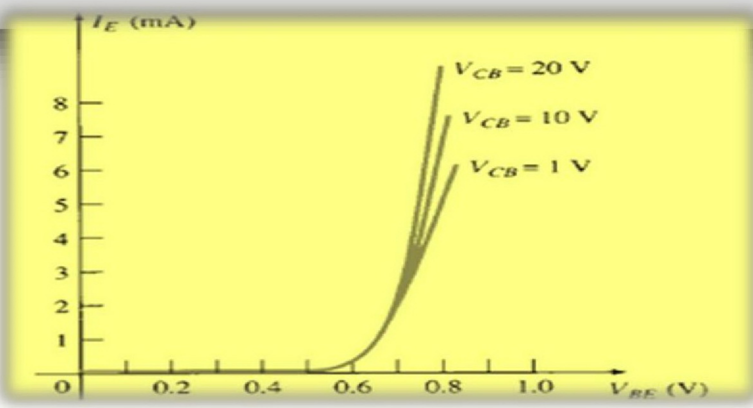
COMMON-BASE CONFIGURATION

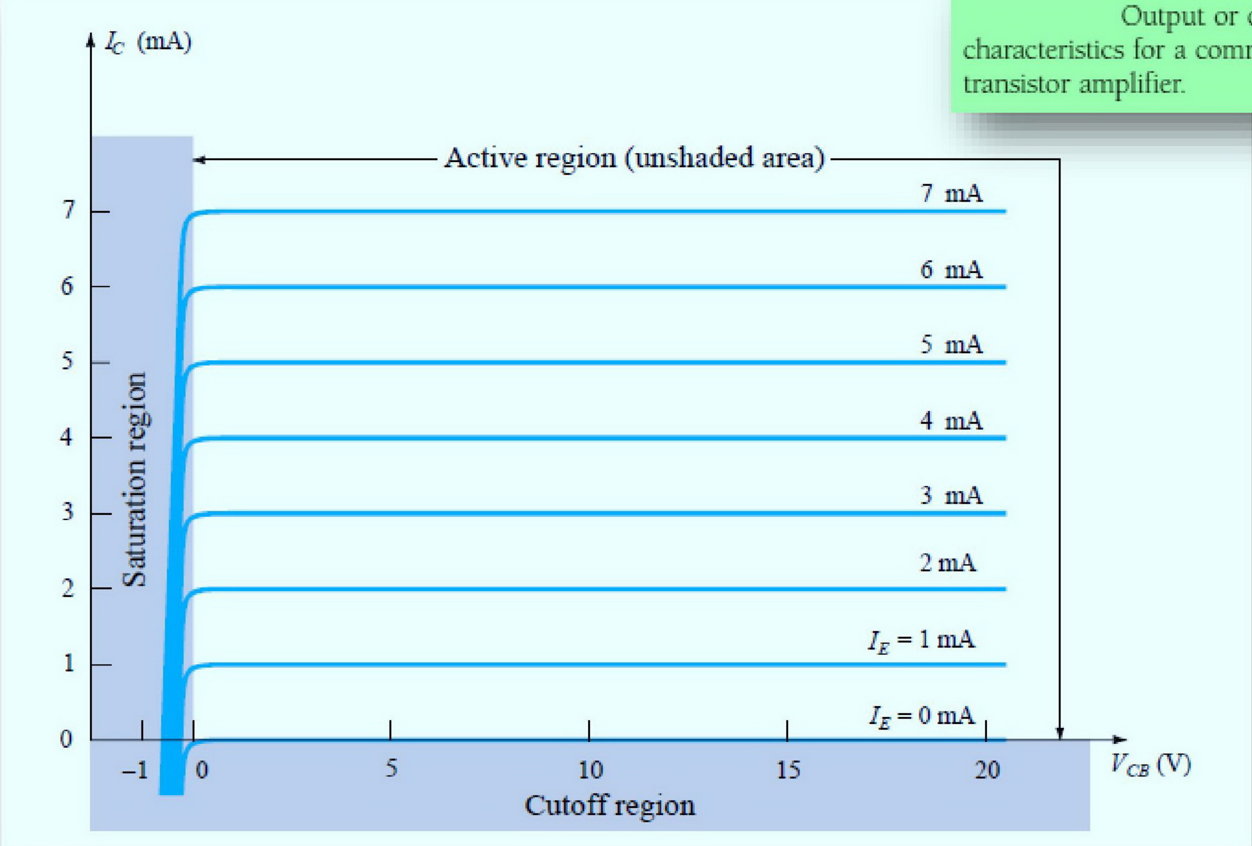
The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential.



The input set for the common-base amplifier as shown in Fig. will relate an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

The output set will relate an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E)





Output or collector characteristics for a common-base transistor amplifier.

In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

In the cutoff region the collector-base and base-emitter junctions of a transistor are both reverse-biased.

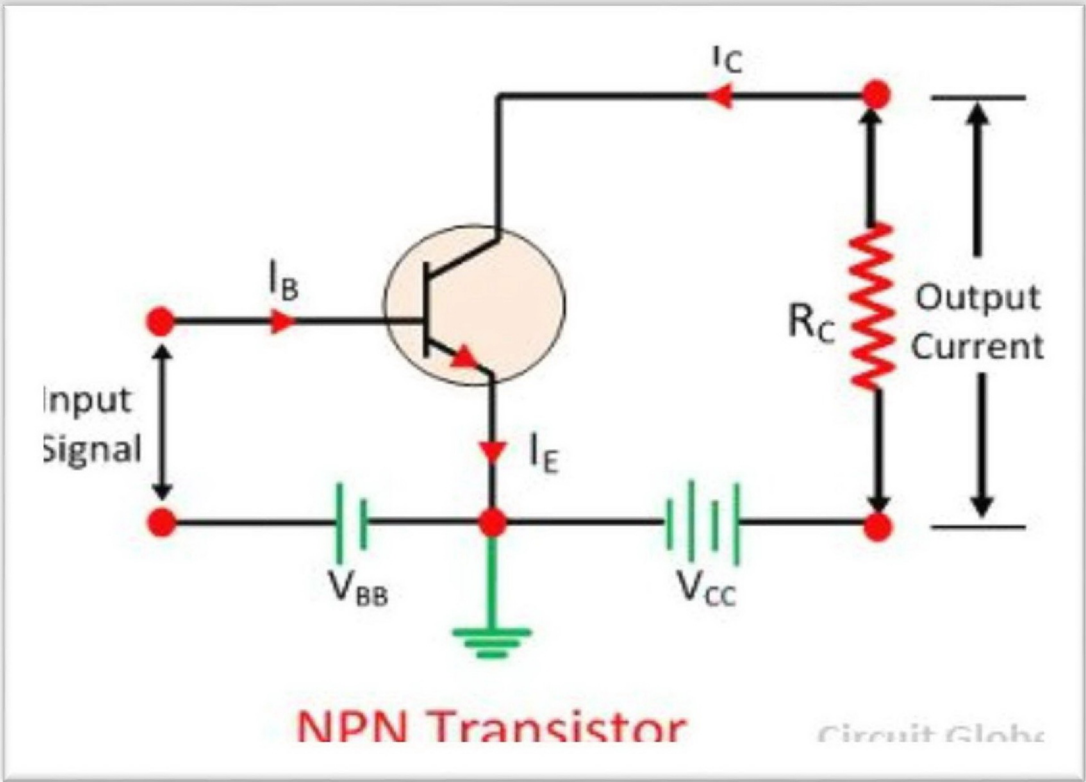
In the saturation region the collector-base and base-emitter junctions are forward-biased.

$$\boxed{I_C \cong I_E}$$

$$\boxed{V_{BE} = 0.7\ \text{V}}$$

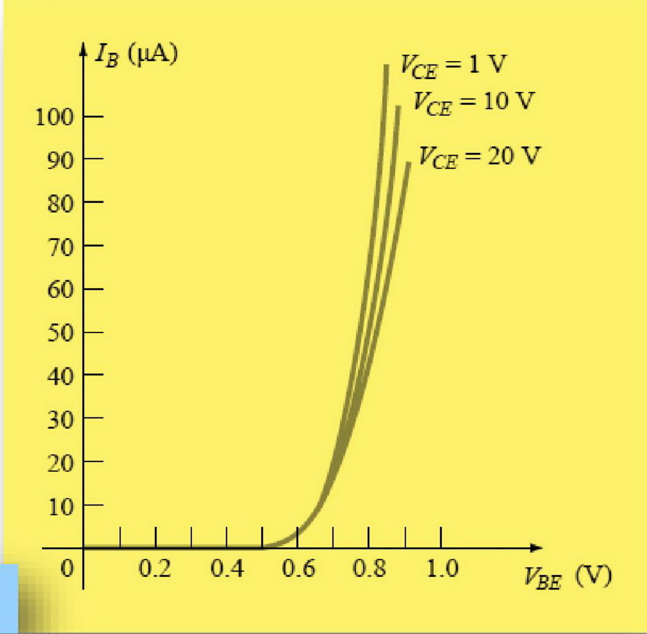
COMMON-EMITTER CONFIGURATION

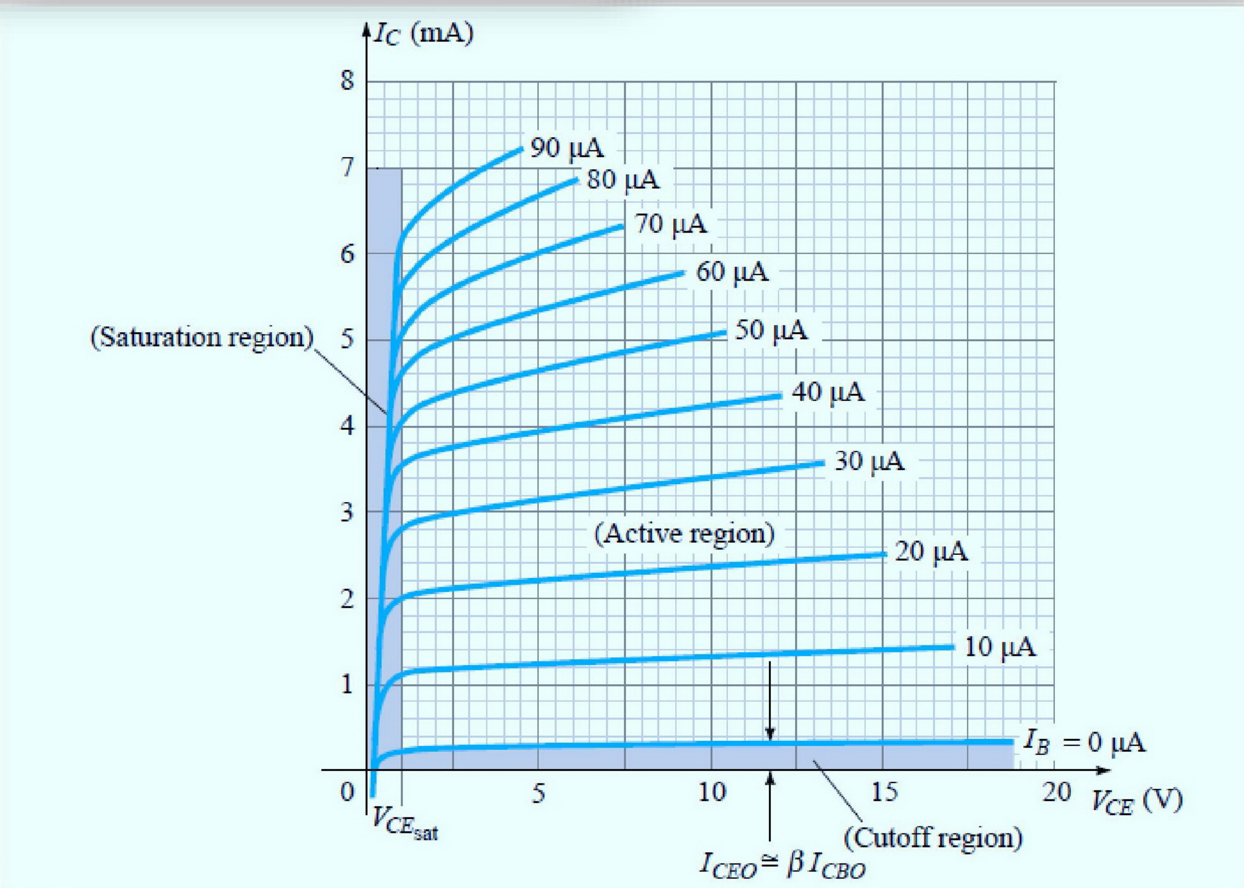
It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals



For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Characteristics of a silicon transistor in the common-emitter config uration:





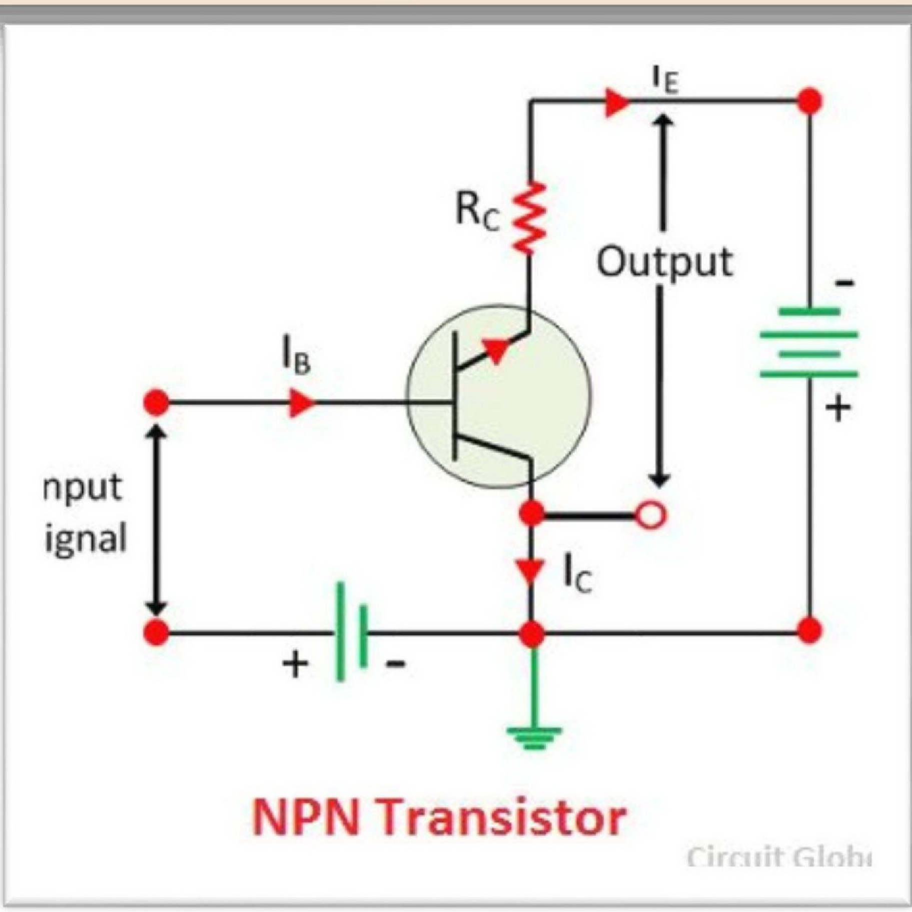
In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

$$\boxed{I_C = \beta I_B}$$

$$\boxed{I_E = (\beta + 1)I_B}$$

COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration,* shown in Fig. with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.



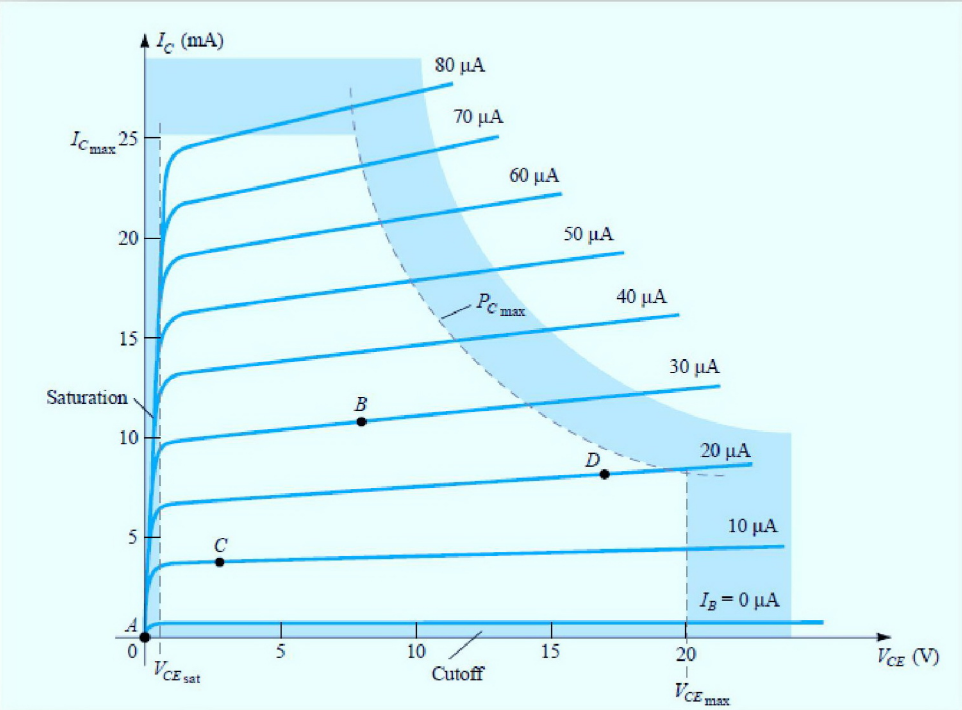
ELECTRONIC DEVICES

4 DC BIASING—BJTS

OPERATING POINT

Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive.

The maximum ratings are indicated on the characteristics of Fig. by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\ \mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{sat}}$.



$$V_{BE} = 0.7\ \text{V}$$

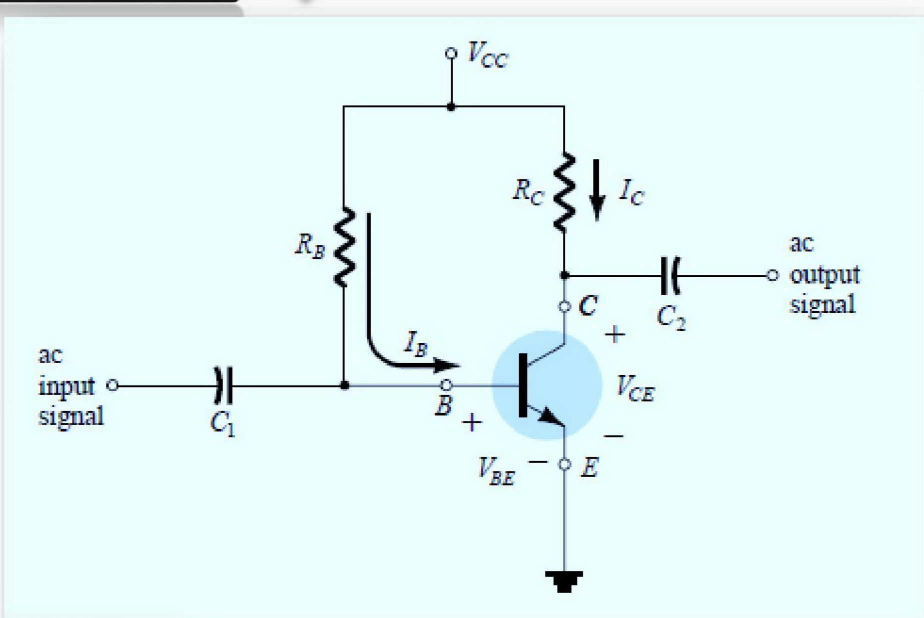
$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

FIXED-BIAS CIRCUIT



$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CE} = V_C - V_E$$

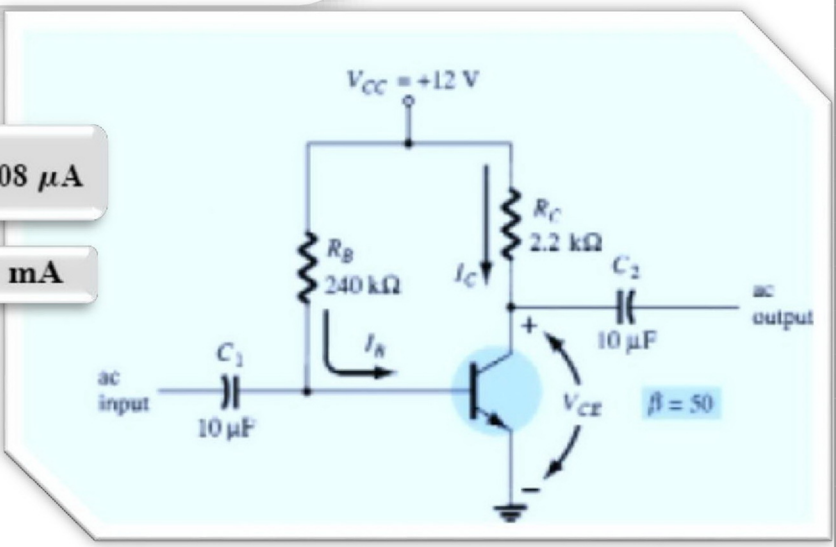
$$V_{CE} = V_C$$

$$V_{BE} = V_B$$

EXAMPLE

Determine the following for the fixed-bias configuration of Fig.
(a) I_{B_Q} and I_{C_Q}.
(b) V_{CE_Q}.
(c) V_B and V_C.
(d) V_{BC}.

Solution



(a) $I_{B_Q} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$

$$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

(b) $V_{CE_Q} = V_{CC} - I_C R_C$
$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$
$= \mathbf{6.83\ V}$

(c) $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

(d) $V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$
$= \mathbf{-6.13\ V}$

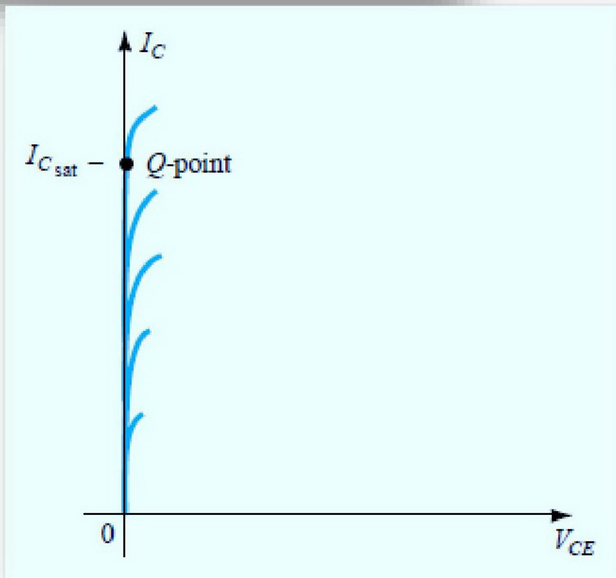
Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values.

the current is relatively high and the voltage V_{CE} is assumed to be zero volts. Applying Ohm's law the resistance between collector and emitter terminals can be determined as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\ \text{V}}{I_{C_{sat}}} = 0\ \Omega$$

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}}$$

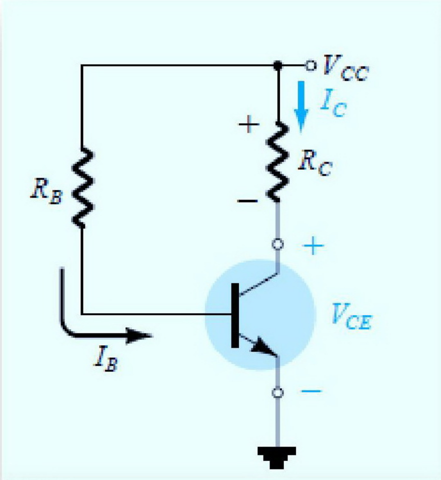


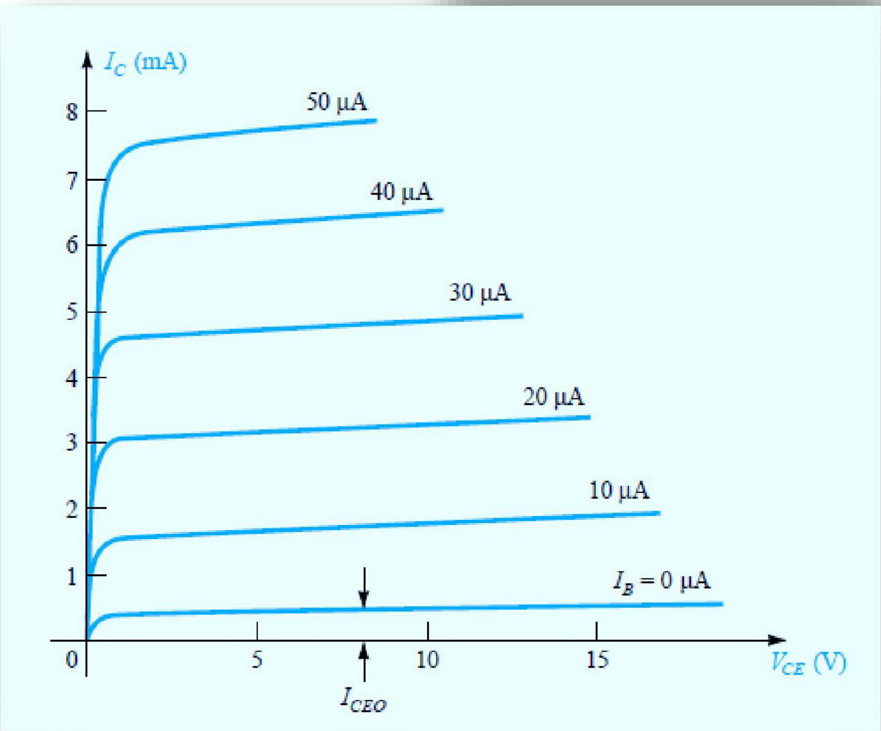
Load-Line Analysis

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC}\,|_{I_C = 0\text{ mA}}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE} = 0\text{ V}}$$

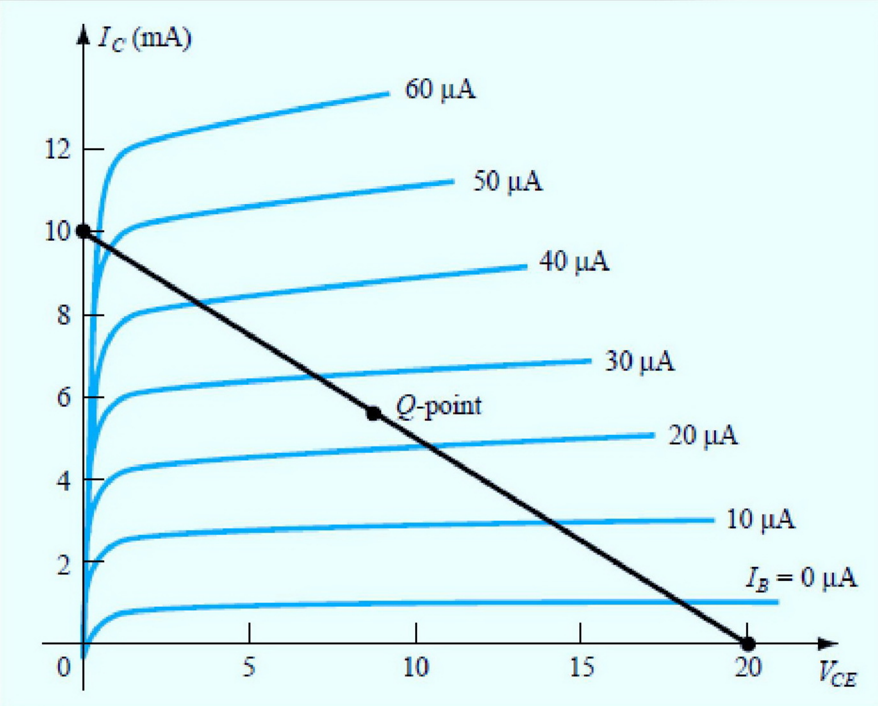




EXAMPLE

Given the load line of Fig.   and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

Solution



$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

EMITTER-STABILIZED BIAS CIRCUIT

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

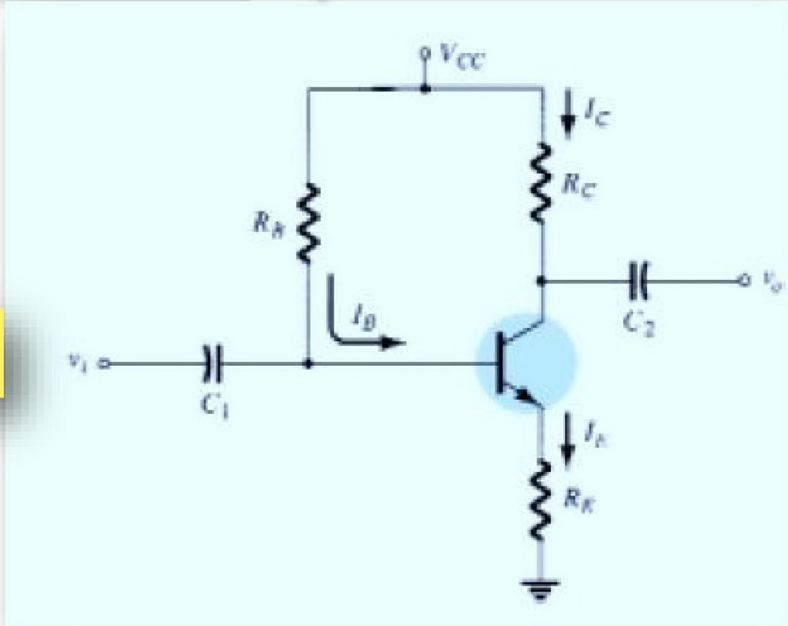
$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B$$

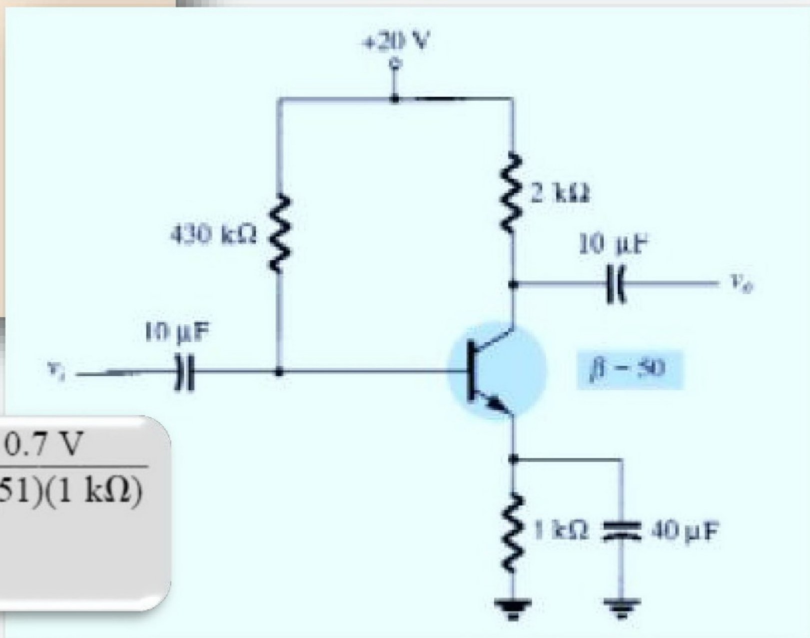
$$V_B = V_{BE} + V_E$$



EXAMPLE

For the emitter bias network of Fig. determine:

(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.
(e) V_E.
(f) V_B.
(g) V_{BC}.



Solution

(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

(c) $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\ V}$$

(d) $$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\ V}$$

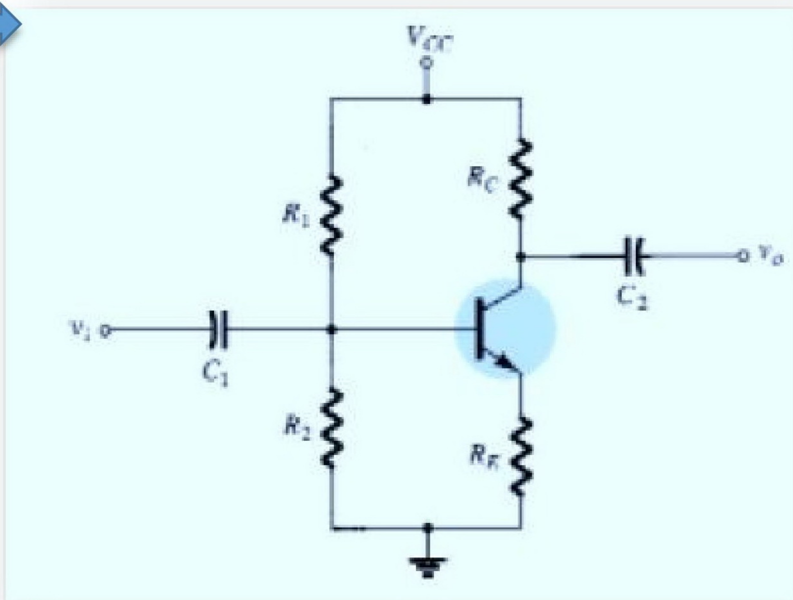
(e) $$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\ V}$$

or $$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\ V}$$

(f) $$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\ V}$$

(g) $$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\ V}$$

VOLTAGE-DIVIDER BIAS



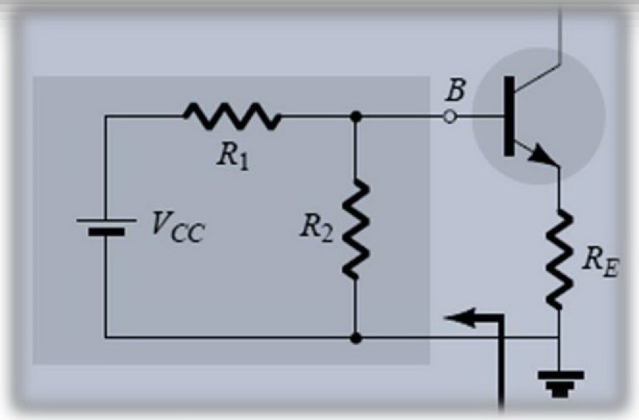
Exact Analysis

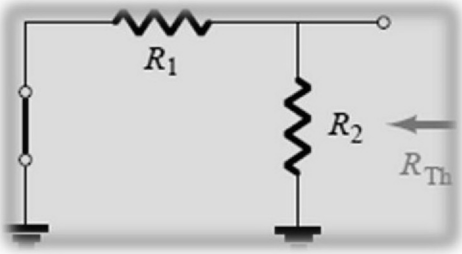
$$\boxed{R_{Th} = R_1 \| R_2}$$

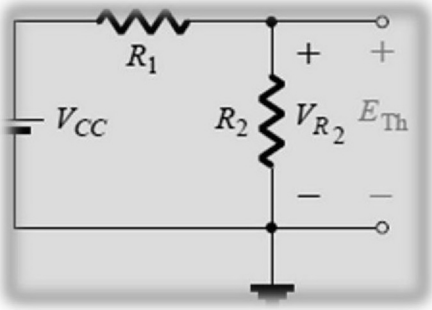
$$\boxed{E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}}$$

$$\boxed{I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}}$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$



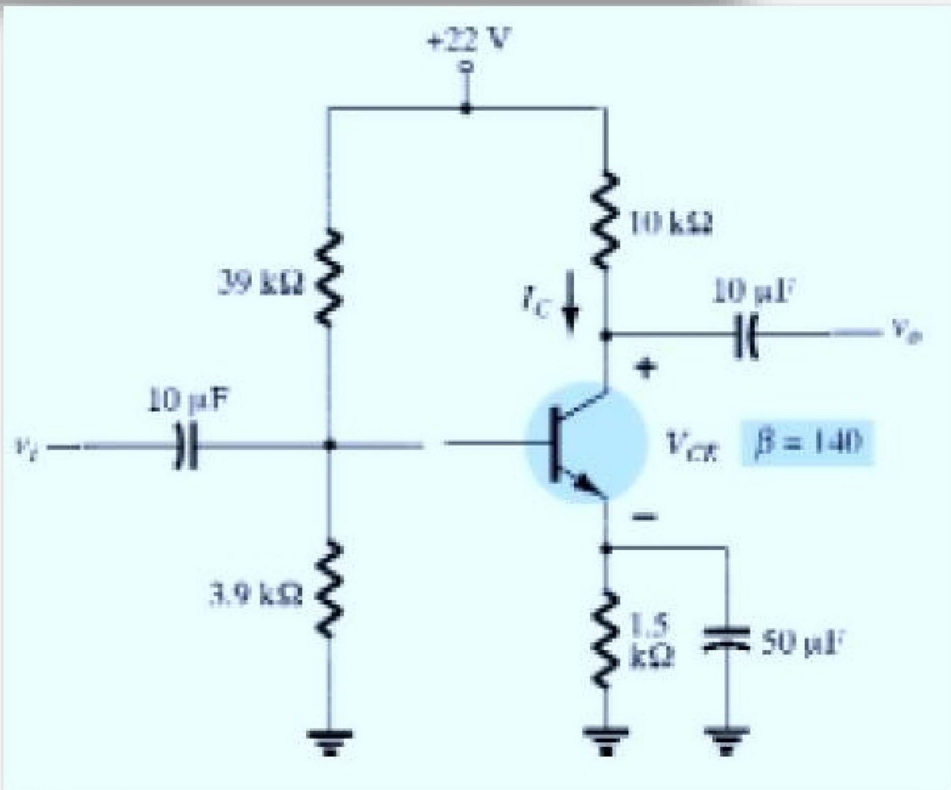




EXAMPLE

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig.

Solution



$$R_{Th} = R_1 \| R_2 = \frac{(39\ \text{k}\Omega)(3.9\ \text{k}\Omega)}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 3.55\ \text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2\ \text{V} - 0.7\ \text{V}}{3.55\ \text{k}\Omega + (141)(1.5\ \text{k}\Omega)} = \frac{1.3\ \text{V}}{3.55\ \text{k}\Omega + 211.5\ \text{k}\Omega} = 6.05\ \mu A$$

$$I_C = \beta I_B$$
$$= (140)(6.05\ \mu A)$$
$$= \mathbf{0.85\ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\ V - (0.85\ mA)(10\ k\Omega + 1.5\ k\Omega)$$
$$= 22\ V - 9.78\ V$$
$$= \mathbf{12.22\ V}$$

Approximate Analysis

$$\boxed{V_B = \frac{R_2 V_{CC}}{R_1 + R_2}}$$

$$\boxed{\beta R_E \geq 10 R_2}$$

$$\boxed{V_E = V_B - V_{BE}}$$

$$\boxed{I_E = \frac{V_E}{R_E}}$$

$$\boxed{I_{C_Q} \cong I_E}$$

$$\boxed{V_{CE_Q} = V_{CC} - I_C(R_C + R_E)}$$

EXAMPLE

Repeat the previous example using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution

$$\beta R_E \geq 10R_2$$
$$(140)(1.5\text{ k}\Omega) \geq 10(3.9\text{ k}\Omega)$$
$$210\text{ k}\Omega \geq 39\text{ k}\Omega \; (\textit{satisfied})$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\text{ k}\Omega)(22\text{ V})}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 2\text{ V}$$

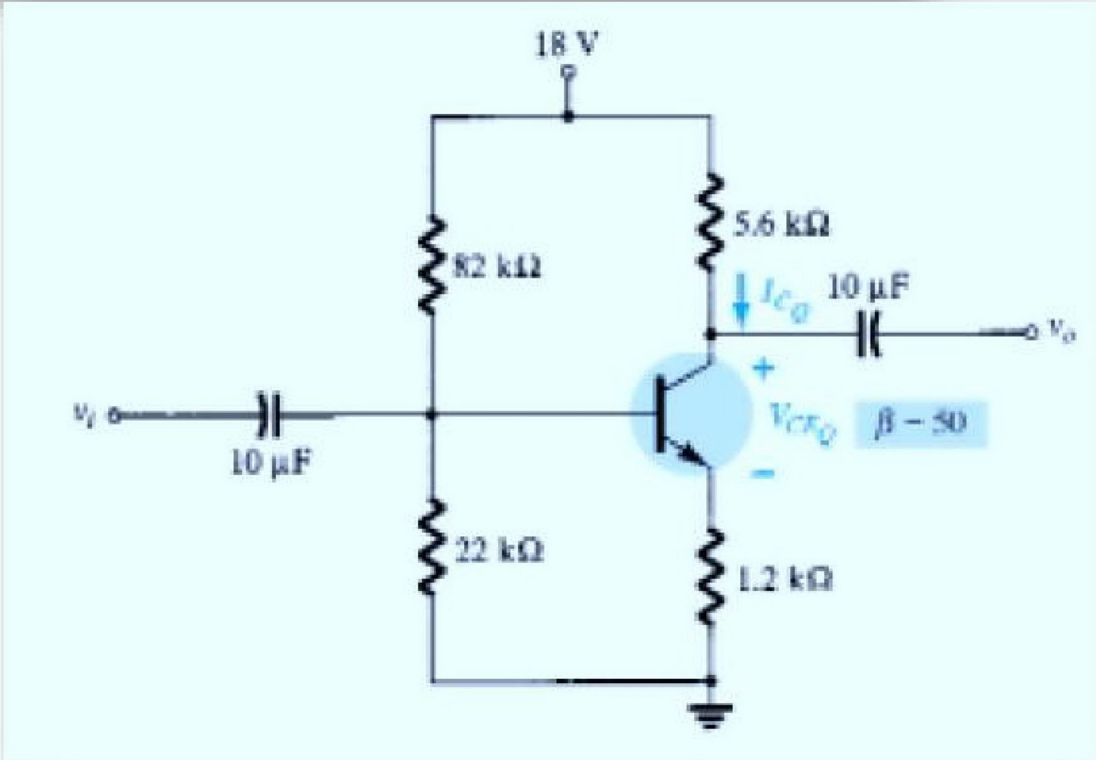
$$V_E = V_B - V_{BE} = 2\text{ V} - 0.7\text{ V} = 1.3\text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.5\text{ k}\Omega} = \mathbf{0.867\text{ mA}}$$

$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 22\text{ V} - (0.867\text{ mA})(10\text{ kV} + 1.5\text{ k}\Omega) \\ &= 22\text{ V} - 9.97\text{ V} \\ &= \mathbf{12.03\text{ V}} \end{aligned}$$

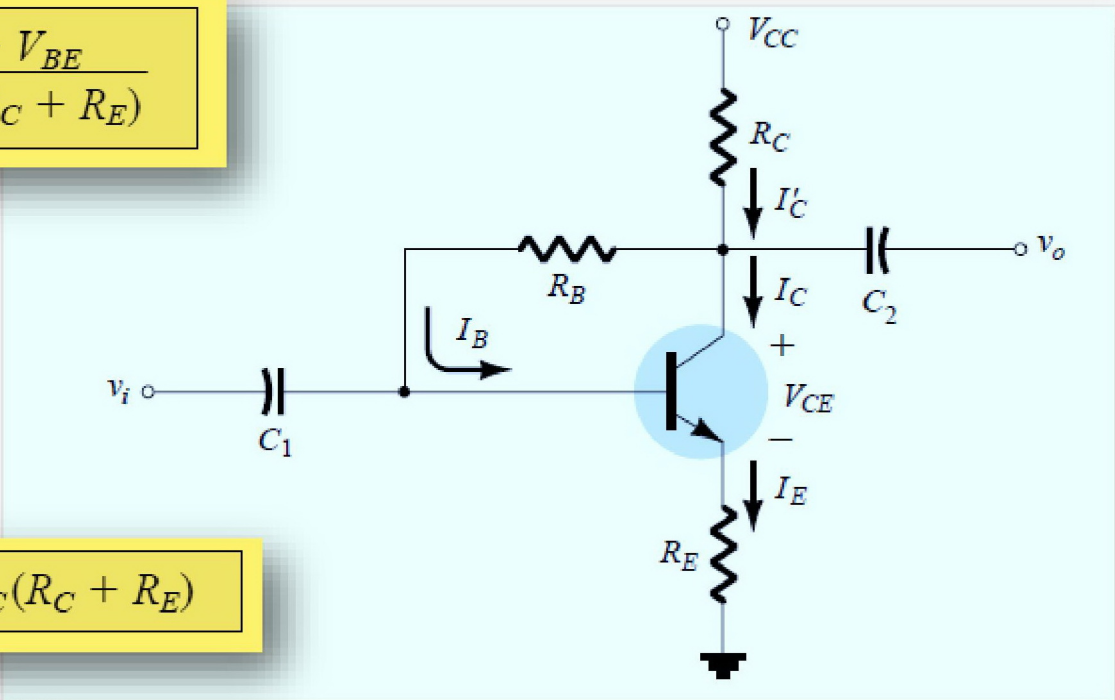
H.W

Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. using the exact and approximate techniques and compare solutions.



DC BIAS WITH VOLTAGE FEEDBACK

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}}$$

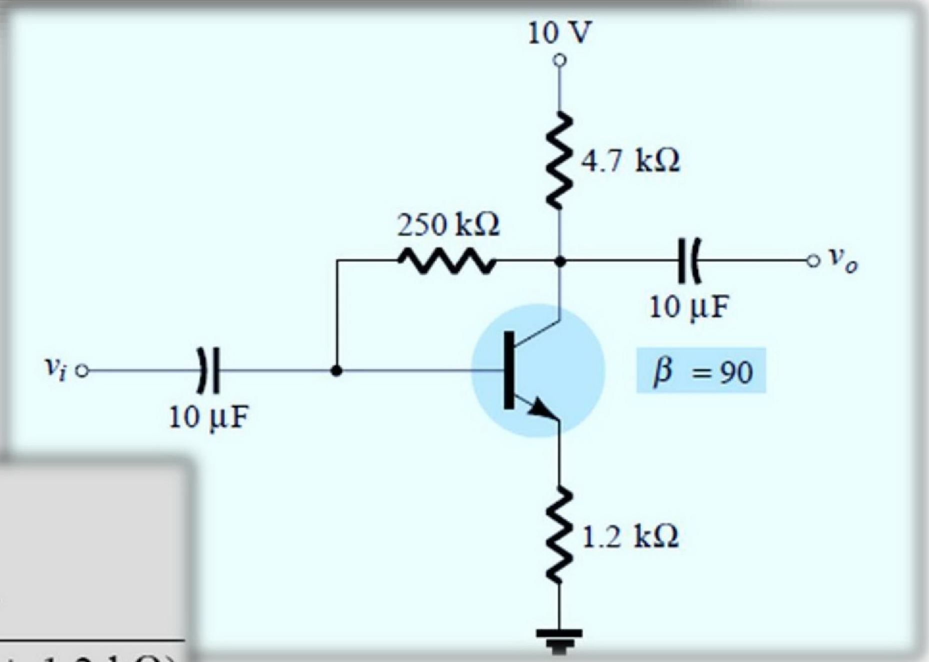


$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

EXAMPLE

Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig.

Solution



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$
$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$
$$= \mathbf{1.07\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 10\text{ V} - 6.31\text{ V}$$
$$= \mathbf{3.69\ V}$$

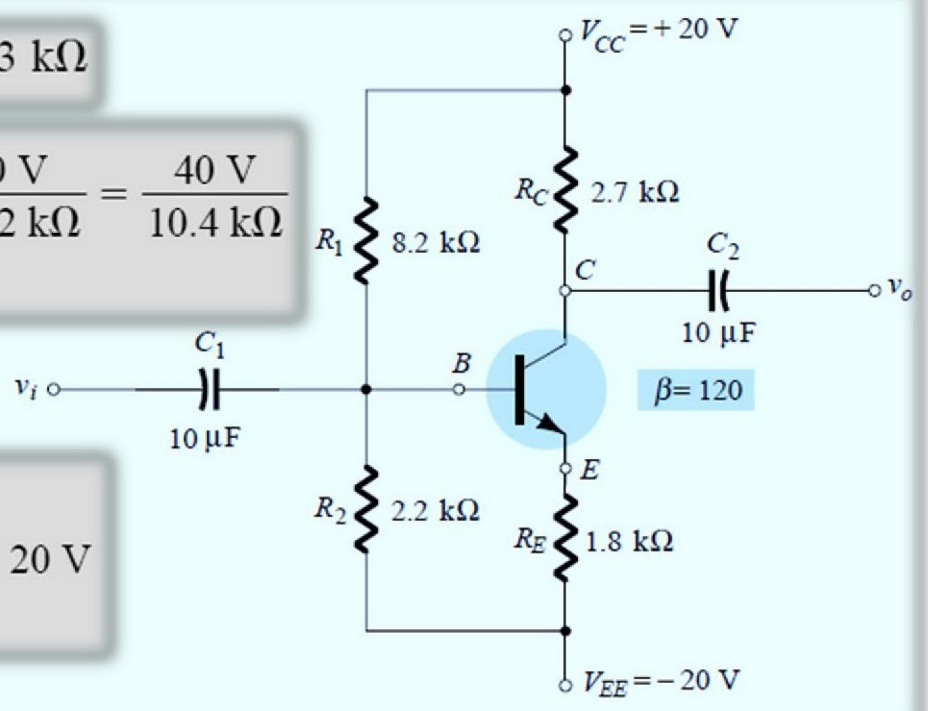
EXAMPLE

Determine V_C and V_B for the network of Fig.

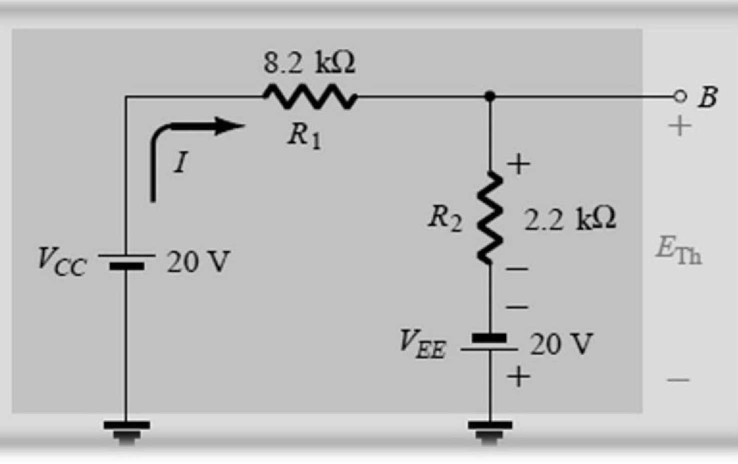
Solution

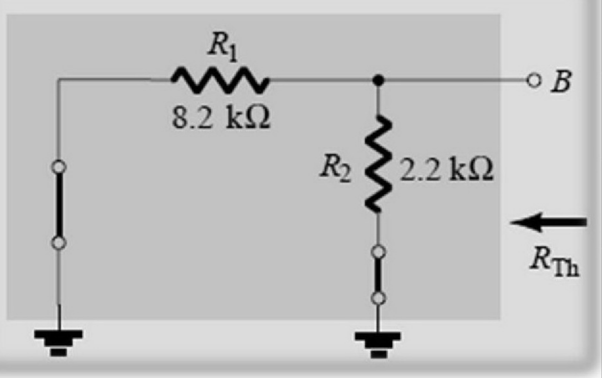
$R_{Th} = 8.2\ k\Omega \| 2.2\ k\Omega = 1.73\ k\Omega$

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\ V + 20\ V}{8.2\ k\Omega + 2.2\ k\Omega} = \frac{40\ V}{10.4\ k\Omega}$$
$$= 3.85\ mA$$

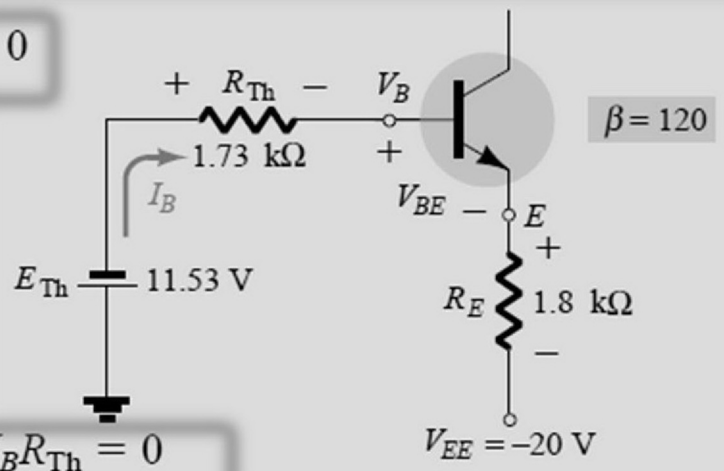


$$E_{Th} = IR_2 - V_{EE}$$
$$= (3.85\ mA)(2.2\ k\Omega) - 20\ V$$
$$= -11.53\ V$$





$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$



$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{20\text{ V} - 11.53\text{ V} - 0.7\text{ V}}{1.73\text{ k}\Omega + (121)(1.8\text{ k}\Omega)}$$

$$= \frac{7.77\text{ V}}{219.53\text{ k}\Omega}$$

$$= 35.39\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (120)(35.39\ \mu\text{A})$$

$$= 4.25\text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (4.25\text{ mA})(2.7\text{ k}\Omega)$$

$$= \mathbf{8.53\ V}$$

$$V_B = -E_{Th} - I_B R_{Th}$$

$$= -(11.53\text{ V}) - (35.39\ \mu\text{A})(1.73\text{ k}\Omega)$$

$$= \mathbf{-11.59\ V}$$

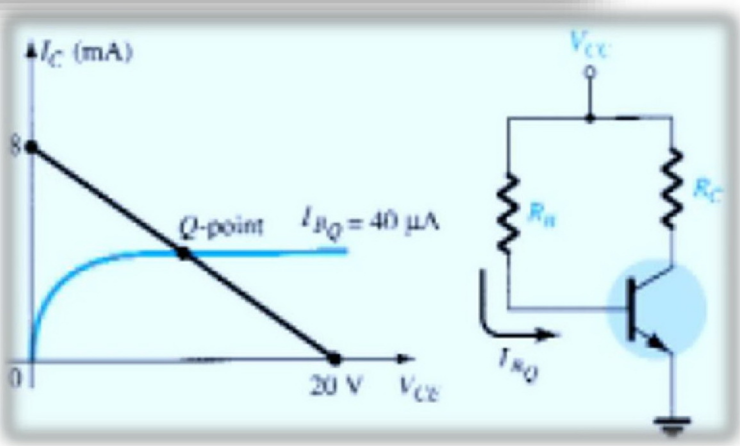
DESIGN OPERATIONS

$$R_{\text{unk}} = \frac{V_R}{I_R}$$

EXAMPLE

Given the device characteristics of Fig. , determine V_{CC}, R_B, and R_C for the fixed-bias configuration

Solution



$V_{CC} = \mathbf{20\ V}$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE} = 0\,\text{V}}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

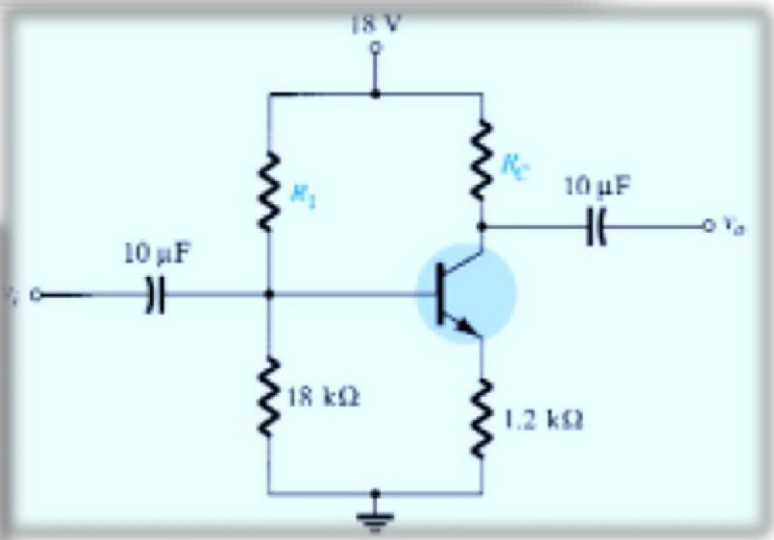
$$= \frac{20\ \text{V} - 0.7\ \text{V}}{40\ \mu\text{A}} = \frac{19.3\ \text{V}}{40\ \mu\text{A}}$$

$$= \mathbf{482.5\ k\Omega}$$

EXAMPLE

Given that $I_{C_Q} = 2$ mA and $V_{CE_Q} = 10$ V, determine R_1 and R_C for the network of Fig

Solution



$$V_E = I_E R_E \cong I_C R_E$$
$$= (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1 \text{ V}$$

$$\frac{(18 \text{ k}\Omega)(18 \text{ V})}{R_1 + 18 \text{ k}\Omega} = 3.1 \text{ V}$$

$$324 \text{ k}\Omega = 3.1 R_1 + 55.8 \text{ k}\Omega$$

$$3.1 R_1 = 268.2 \text{ k}\Omega$$

$$R_1 = \frac{268.2 \text{ k}\Omega}{3.1} = \mathbf{86.52 \text{ k}\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

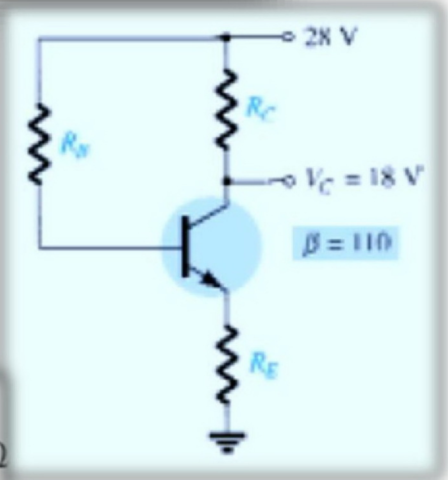
$$V_C = V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V}$$

$$R_C = \frac{18 \text{ V} - 12.4\text{V}}{2\text{mA}}$$

$$= \mathbf{2.8 \text{ k}\Omega}$$

EXAMPLE

The emitter-bias configuration of Fig. has the following specifications: $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$, $I_{C_{sat}} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C, R_E, and R_B.



Solution

$$I_{C_Q} = \tfrac{1}{2}I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}} = \frac{28\text{ V} - 18\text{ V}}{4\text{ m}A} = \mathbf{2.5\ k\Omega}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28\text{ V}}{8\text{ mA}} = 3.5\text{ k}\Omega$$

$$R_E = 3.5\text{ k}\Omega - R_C = 3.5\text{ k}\Omega - 2.5\text{ k}\Omega = \mathbf{1\ k\Omega}$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4\text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

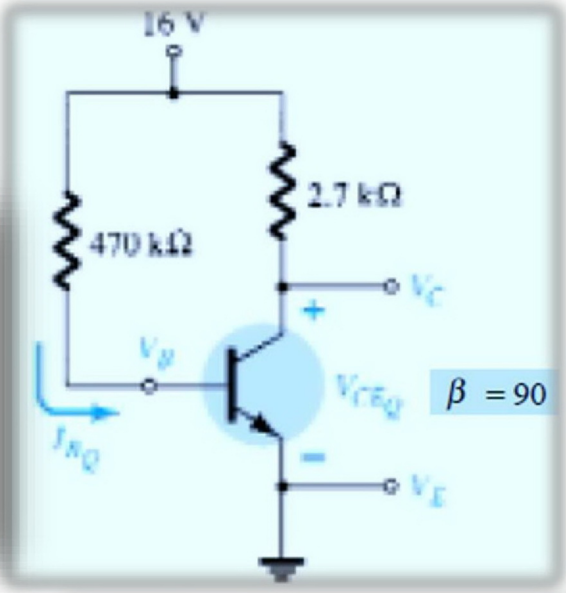
$$= \frac{28\text{ V} - 0.7\text{ V}}{36.36\ \mu\text{A}} - (111)(1\text{ k}\Omega)$$

$$= \frac{27.3\text{ V}}{36.36\ \mu\text{A}} - 111\text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

Exercises

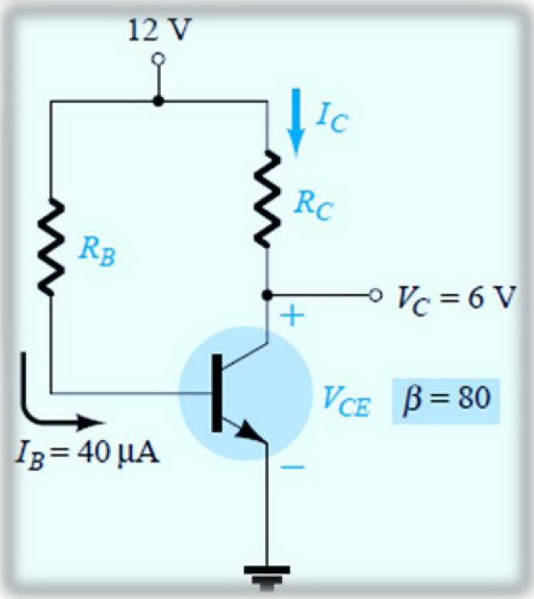
1.



For the fixed-bias configuration of Fig. , determine:

(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_B.
(f) V_E.

2.

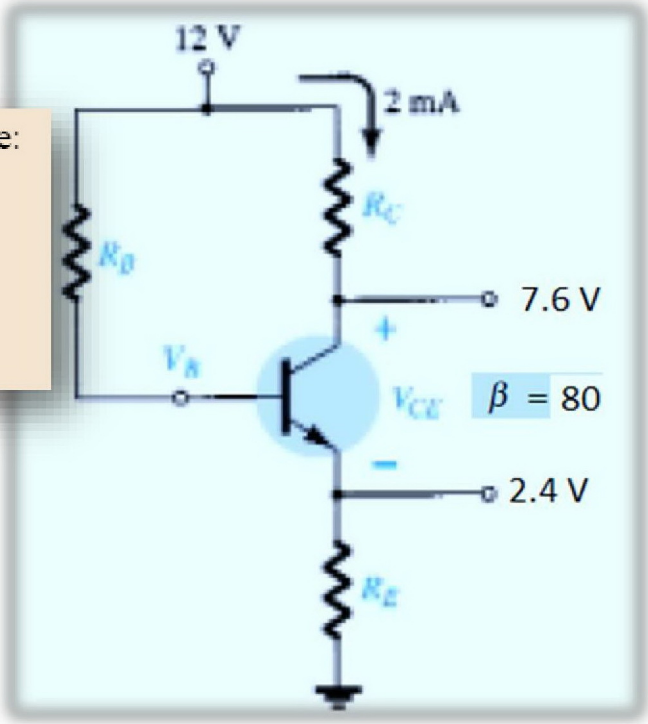


Given the information appearing in Fig. , determine:

(a) I_C.
(b) R_C.
(c) R_B.
(d) V_{CE}.

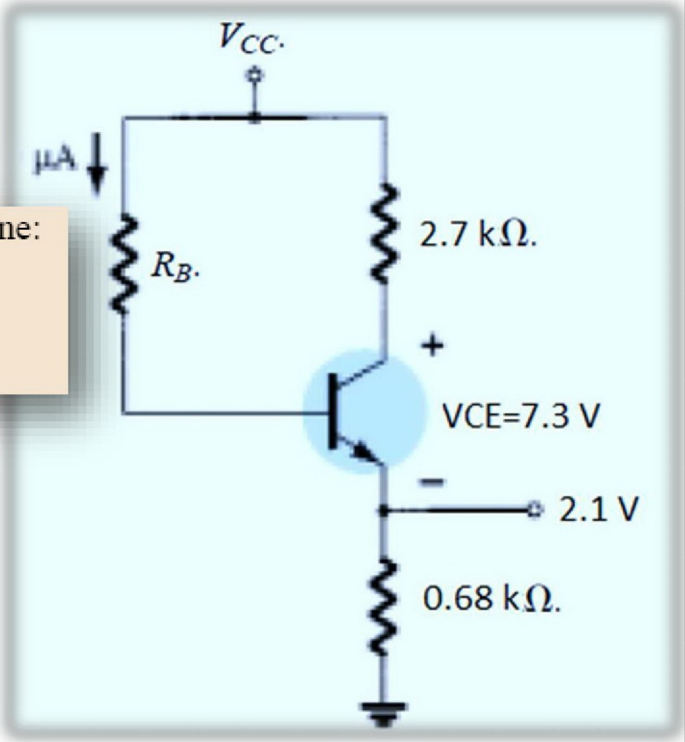
3.

Given the information provided in Fig. , determine:
(a) R_C.
(b) R_E.
(c) R_B.
(d) V_{CE}.
(e) V_B.



4.

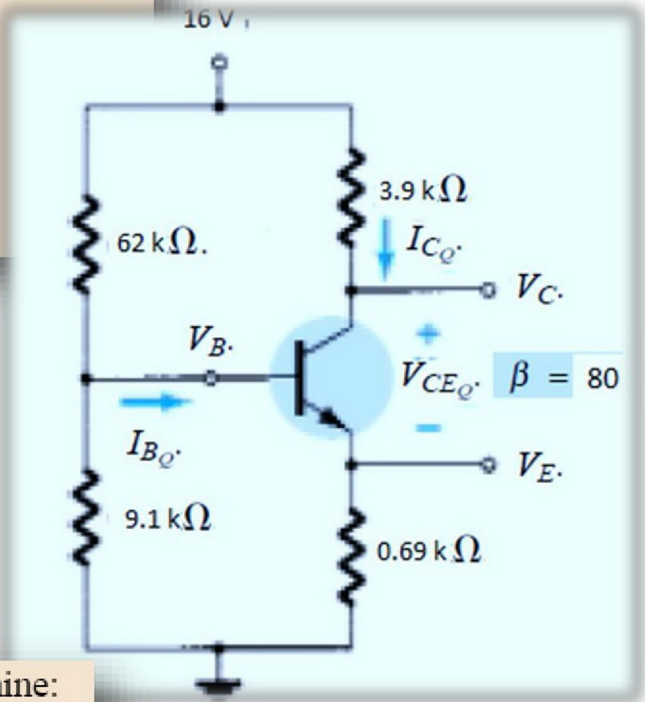
Given the information provided in Fig. determine:
(a) β.
(b) V_{CC}.
(c) R_B.



5.

For the voltage-divider bias configuration of Fig.   determine:

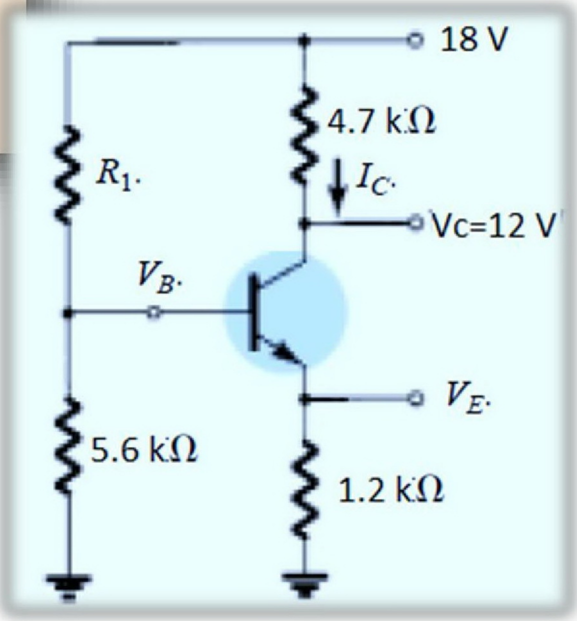
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_E.
(f) V_B.



6.

Given the information provided in Fig.   , determine:

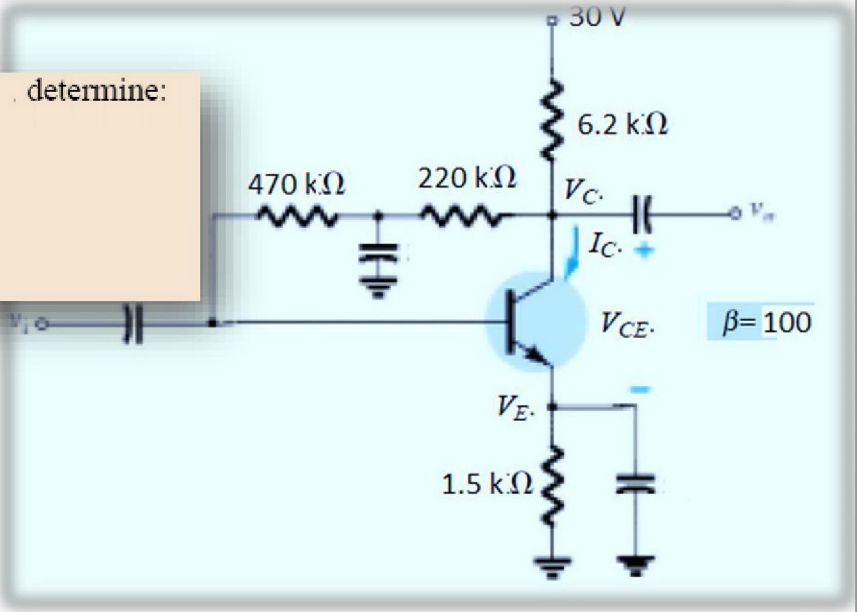
(a) I_C.
(b) V_E.
(c) V_B.
(d) R_1.



7.

For the voltage feedback network of Fig. determine:

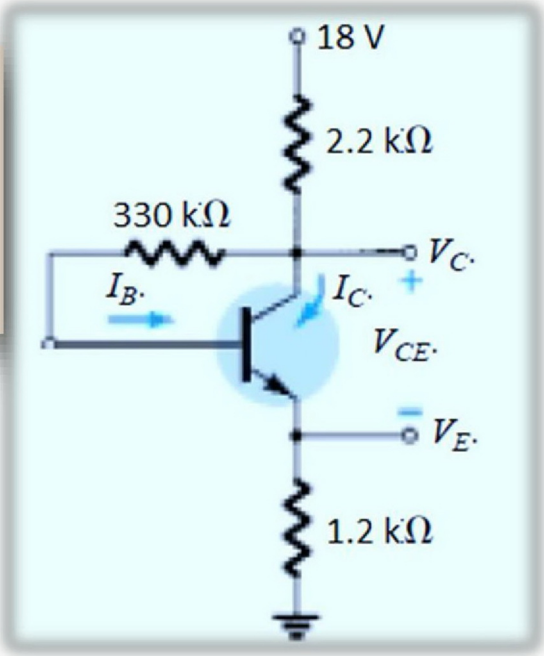
(a) I_C.
(b) V_C.
(c) V_E.
(d) V_{CE}.



8.

Given $V_B = 4$ V for the network of Fig. , determine:

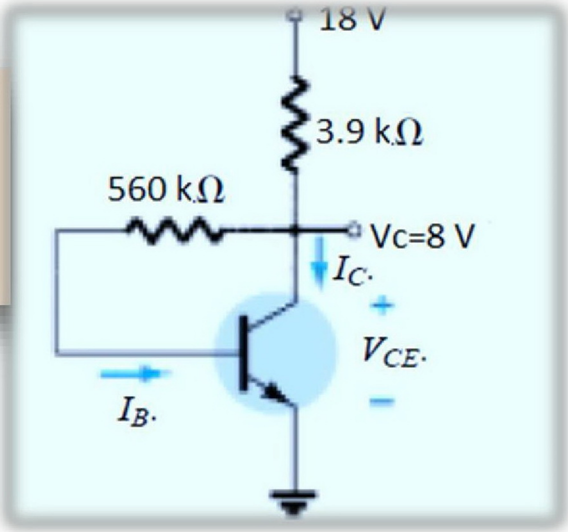
(a) V_E.
(b) I_C.
(c) V_C.
(d) V_{CE}.
(e) I_B.



9.

Given $V_C = 8$ V for the network of Fig. , determine:

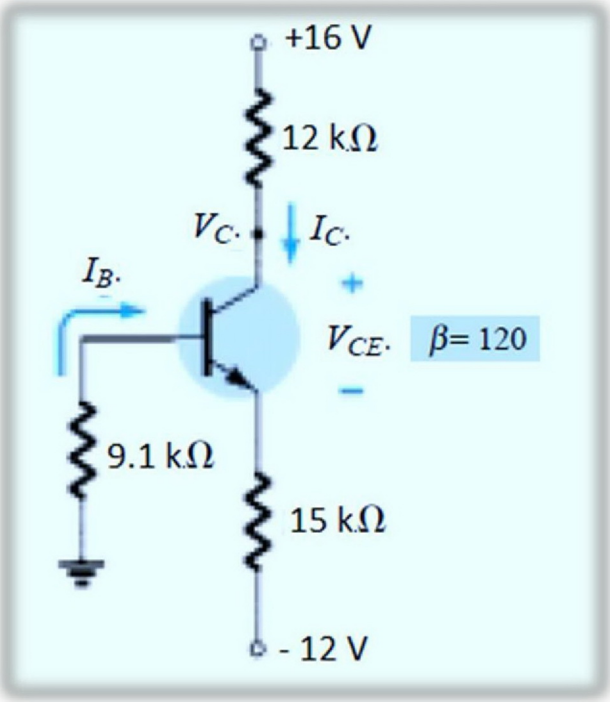
(a) I_B.
(b) I_C.
(c) β.
(d) V_{CE}.

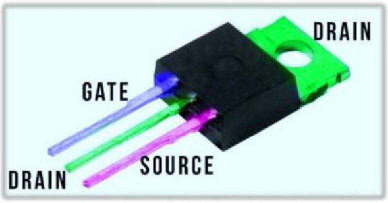


10.

For the network of Fig. , determine:

(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.





ELECTRONIC DEVICES

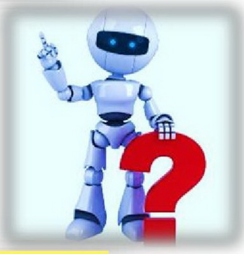
5 FIELD-EFFECT TRANSISTORS

Basic Definitions:

The FET is a semiconductor device whose operation consists of controlling the flow of current through a semiconductor channel by application of an electric field (voltage).

There are two categories of FETs: the ***junction field-effect transistor*** (JFET) and the ***metal-oxide-semiconductor field-effect transistor*** (MOSFET). The MOSFET category is further broken-down into: ***depletion*** and ***enhancement*** types.

A Comparison between FET and BJT:

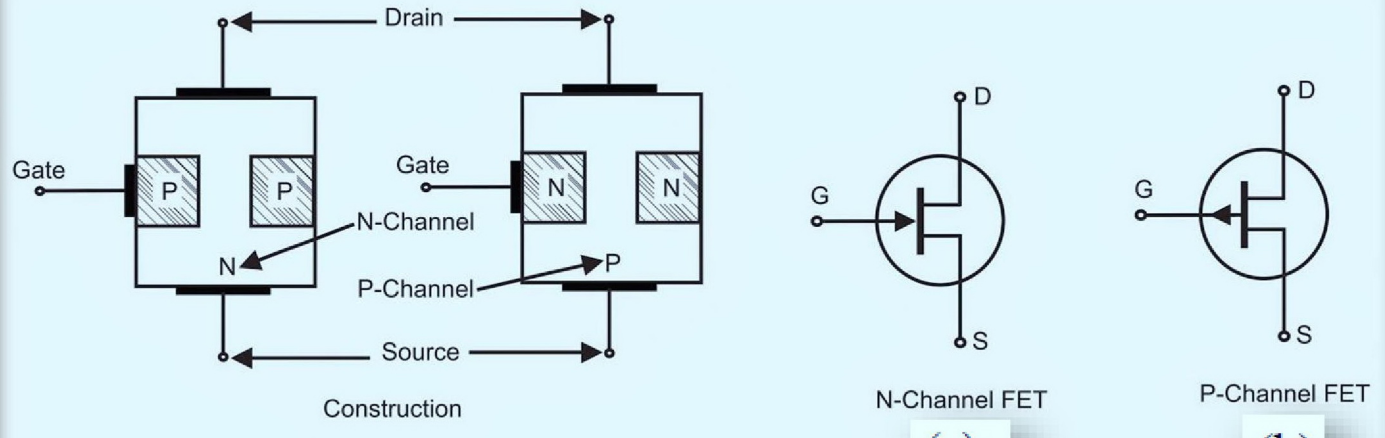


- FET is a ***unipolar*** device. It operates as a ***voltage-controlled*** device with either electron current in an ***n-channel*** FET or hole current in a ***p-channel*** FET.
- BJT made as ***npn*** or as ***pnp*** is a ***current-controlled*** device in which both electron current and hole current are involved.
- The FET is smaller than a BJT and is thus for more popular in ***integrated circuits*** (ICs).

- FETs exhibit much higher ***input impedance*** than BJTs.
- FETs are more ***temperature stable*** than BJTs.
- BJTs have large ***voltage gain*** than FETs when operated as an amplifier.
- The BJT has a much higher ***sensitivity*** to changes in the applied signal (faster ***response***) than a FET.

Junction Field-Effect Transistor (JFET):

The basic construction of n-channel (p-channel) JFET is shown in Fig. a (b). Note that the major part of the structure is n-type (p-type) material that forms the channel between the embedded layers of p-type (n-type) material. The top of the n-type (p-type) channel is connected through an ohmic contact to a terminal referred to as the ***drain*** "D", while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the ***source*** "S". The two p-type materials are connected together and to the ***gate*** "G" terminal.

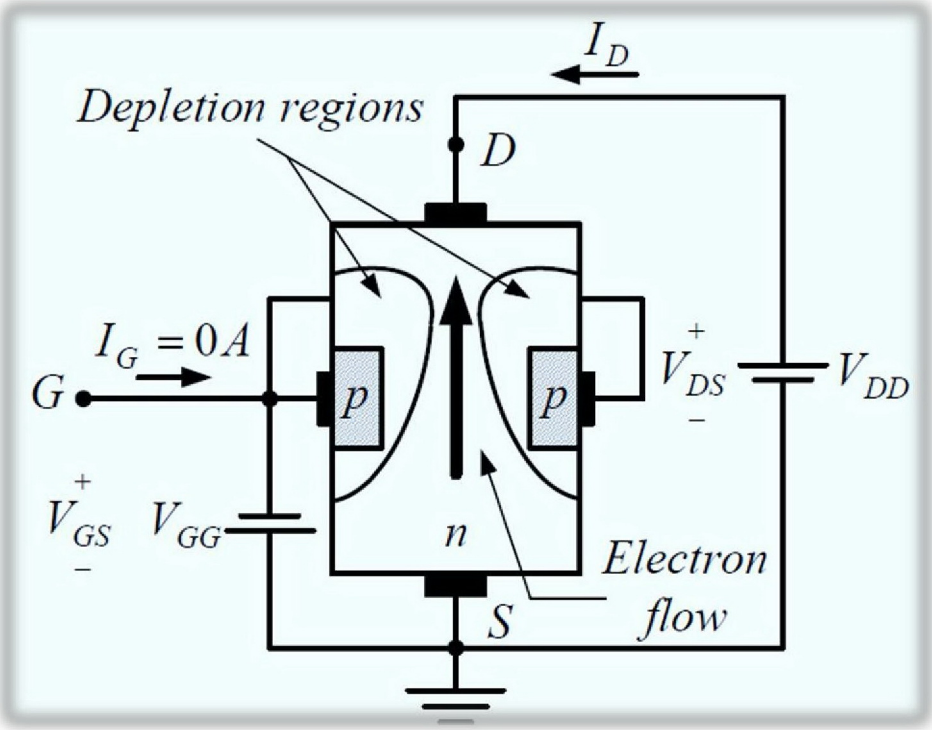


(a) (b)

Construction and symbols for FET's

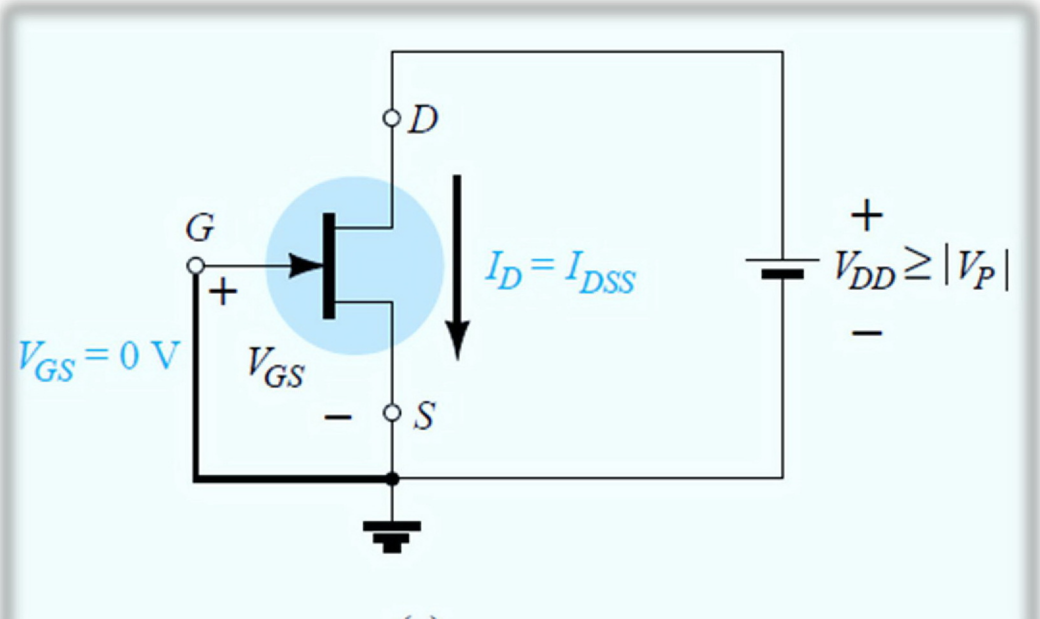
Basic Operation of JFET:

- Bias voltages are shown, in Fig. below applied to an n-channel JFET devise.
- V_{DD} provides a drain-to-source voltage, V_{DS}, (drain is positive relative to source) and supplies current from drain to source, I_D, (electrons move from source to drain).
- V_{GG} sets the reverse-bias voltage between the gate and the source, V_{GS}, (gate is biased negative relative to the source).
- Input impedance at the gate is very high, thus the gate current $I_G = 0$ A.
- Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus increases its resistance.
- The channel width can be controlled by varying the gate voltage, and thereby, I_D can also be controlled.
- The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is grater than that between the gate and the source.

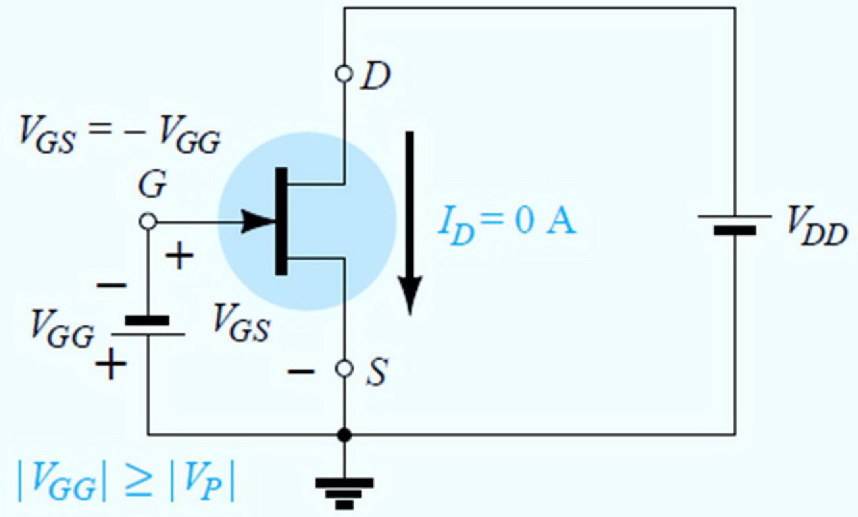


JFET Characteristics:

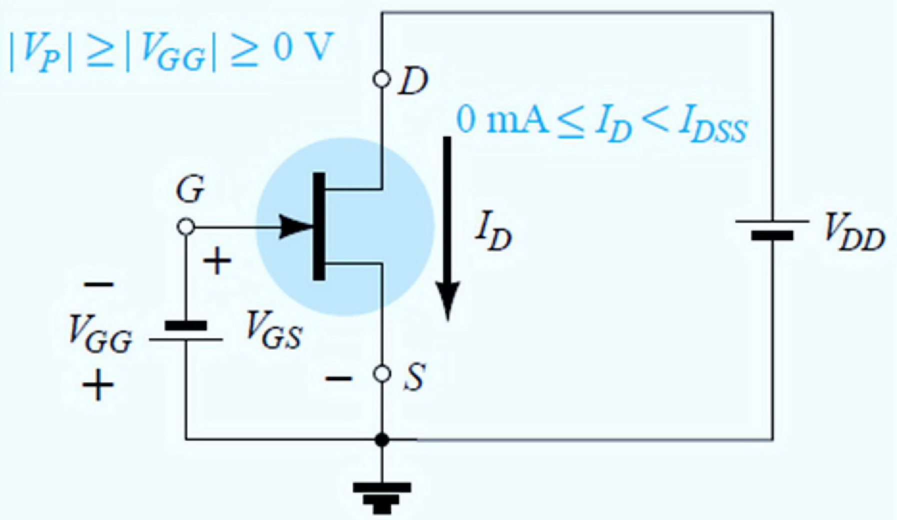
- The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$ as shown in Fig.a.
- For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A) as appearing in Fig. b.
- For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as reviewed by Fig. c.
  For p-channel JFETs a similar list can be developed.



(a)


D
$V_{GS} = -V_{GG}$
G
$I_D = 0$ A
V_{DD}
+
−
V_{GG}
V_{GS}
+
−
S
$|V_{GG}| \geq |V_P|$

(b)


$|V_P| \geq |V_{GG}| \geq 0$ V
D
0 mA $\leq I_D < I_{DSS}$
G
I_D
V_{DD}
+
−
V_{GG}
V_{GS}
+
−
S

(c)

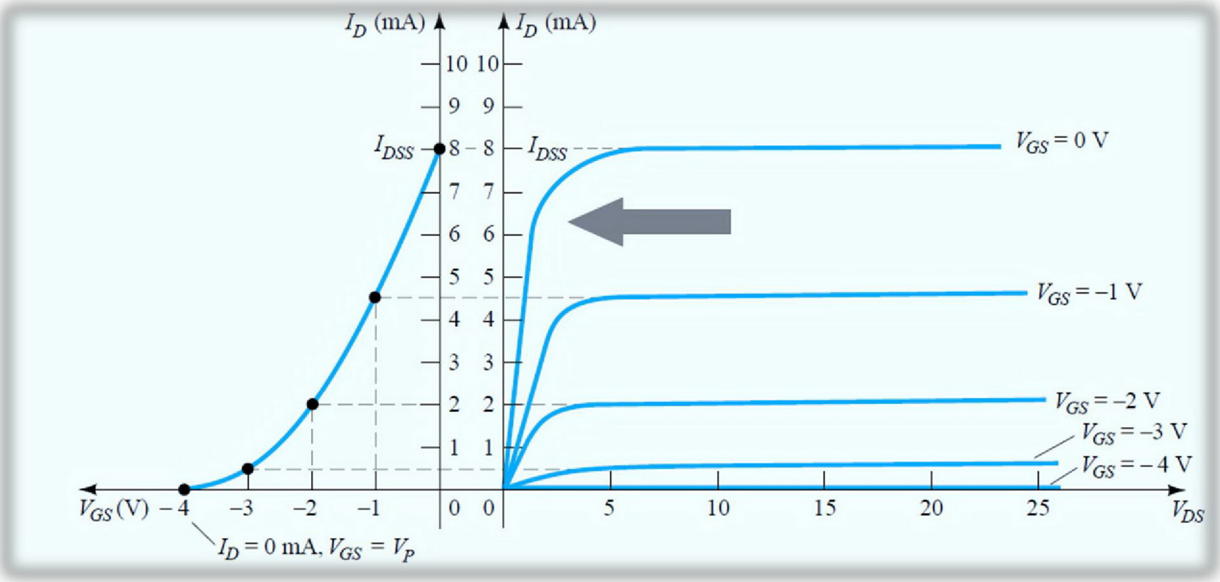
Shockley's Equation:

$$\boxed{I_C = f(I_B) = \underbrace{\beta}_{\text{constant}} \overbrace{I_B}^{\text{control variable}}}$$

$$\boxed{I_D = \underbrace{I_{DSS}}_{\text{constants}}\left(1 - \frac{\overbrace{V_{GS}}^{\text{control variable}}}{\underbrace{V_P}_{\text{constants}}}\right)^2}$$

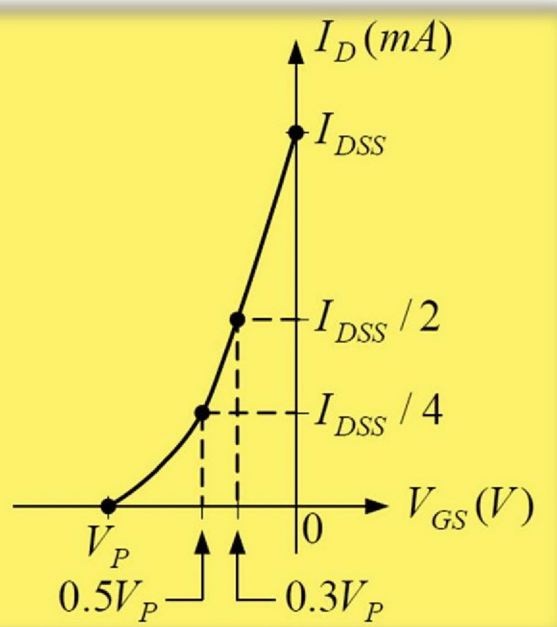
TRANSFER CHARACTERISTICS

Transfer characteristics are plots of I_D versus V_{GS} for a fixed value of V_{DS}. The transfer curve can be obtained from the output characteristics as shown in Fig. , or it can be sketched to a satisfactory level of accuracy (see Fig.) simply using Shockley's equation with the four plot points defined in Table below.

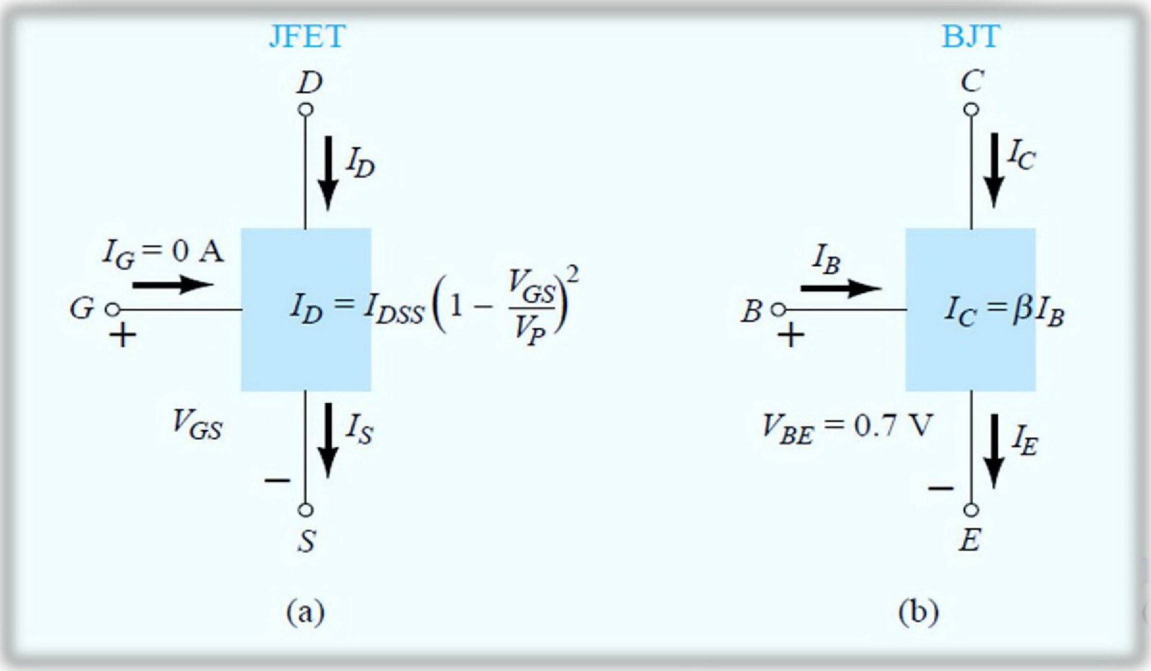


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_{GS} (V)	I_D (mA)
0	I_{DSS}
0.3 V_P	I_{DSS} / 2
0.5 V_P	I_{DSS} / 4
V_P	0



Important Relationships:



JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0A$	$\Leftrightarrow$	$V_{BE} \cong 0.7V$

EXAMPLE

Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution

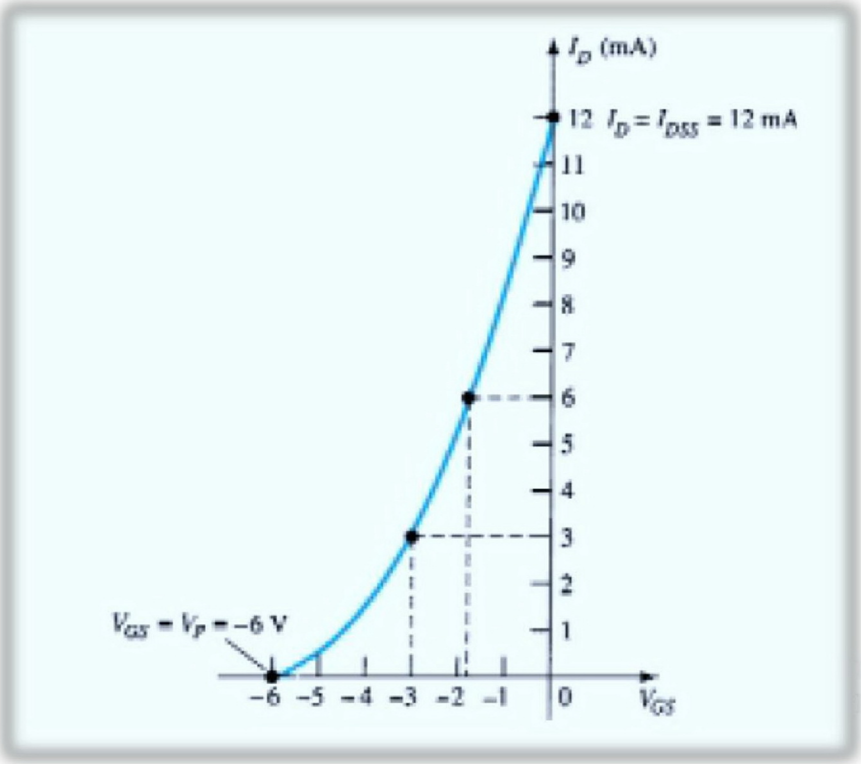
Two plot points are defined by

$$I_{DSS} = \mathbf{12\ mA} \qquad \text{and} \qquad V_{GS} = \mathbf{0\ V}$$

and

$$I_D = \mathbf{0\ mA} \qquad \text{and} \qquad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\ V}$ the drain current will be determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\ mA}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\ V}$. All four plot points are well defined on Fig. 5.16 with the complete transfer curve.



6 FET BIASING

FIXED-BIAS CONFIGURATION

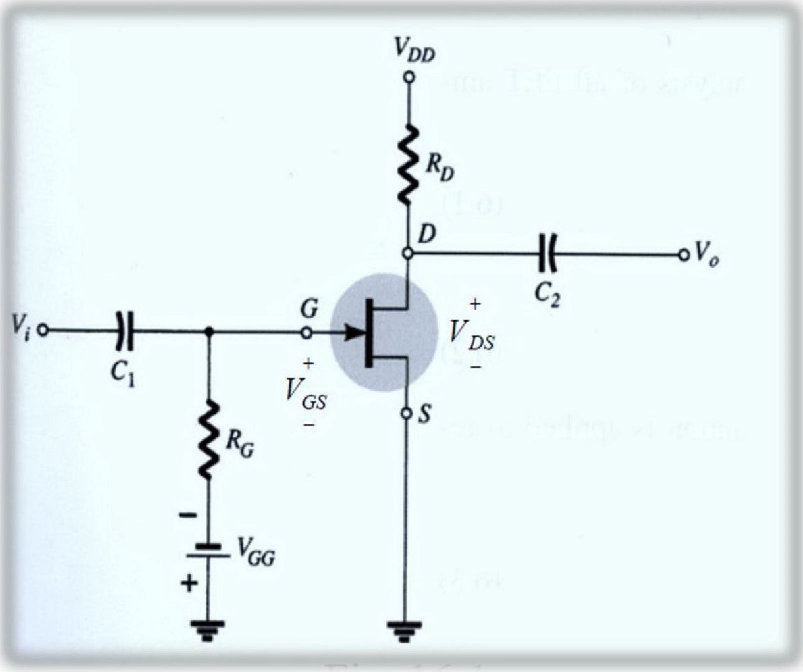
$$\boxed{V_{GS} = -V_{GG}}$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

$$\boxed{V_S = 0\ \text{V}}$$

$$\boxed{V_D = V_{DS}}$$

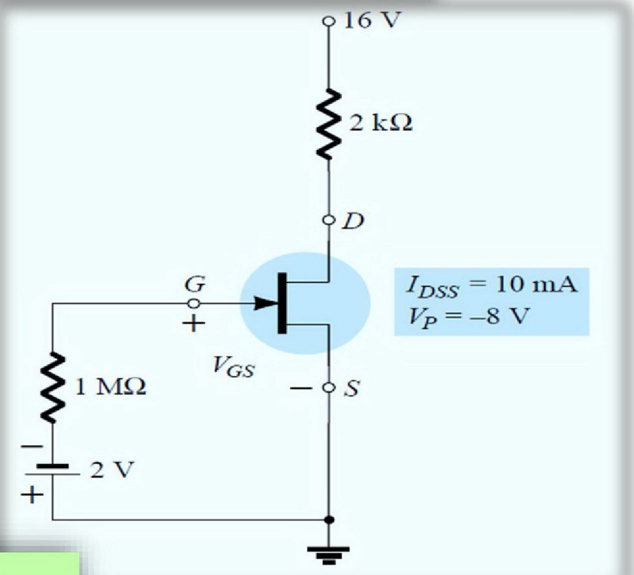
$$\boxed{V_G = V_{GS}}$$



EXAMPLE

Determine the following for the network of Fig.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.



Solution

Mathematical Approach:

a) $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

(b) $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

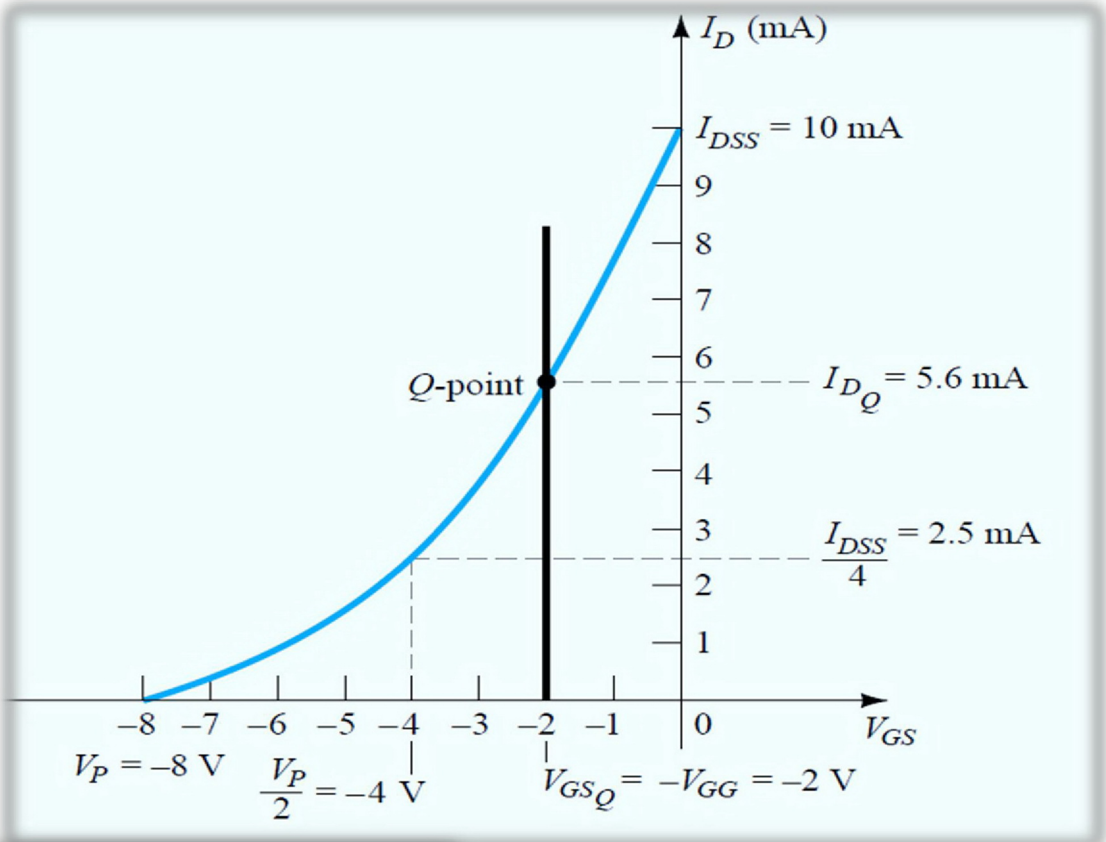
(c) $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Graphical Approach:



$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$

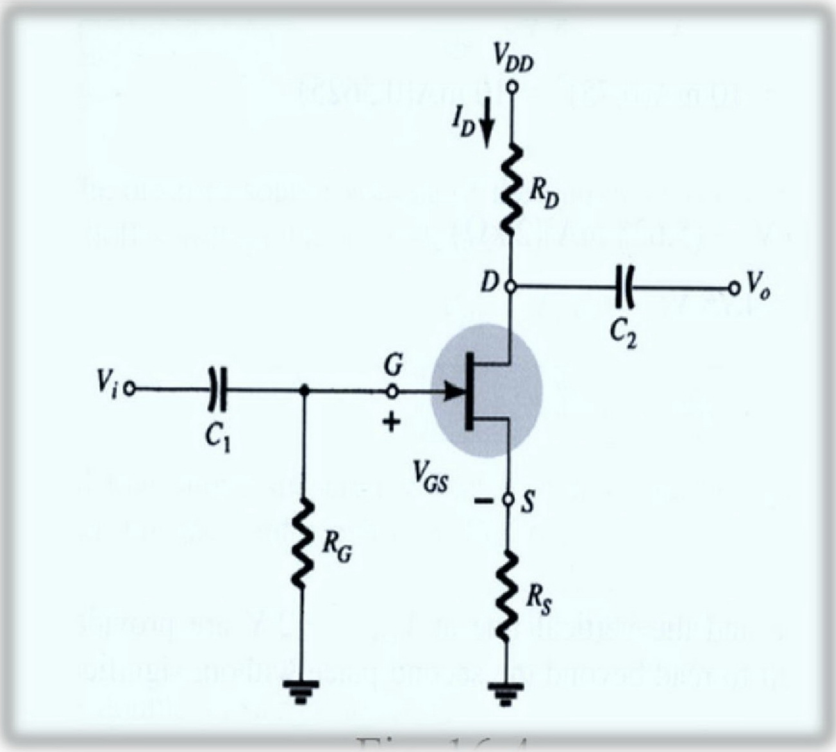
(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

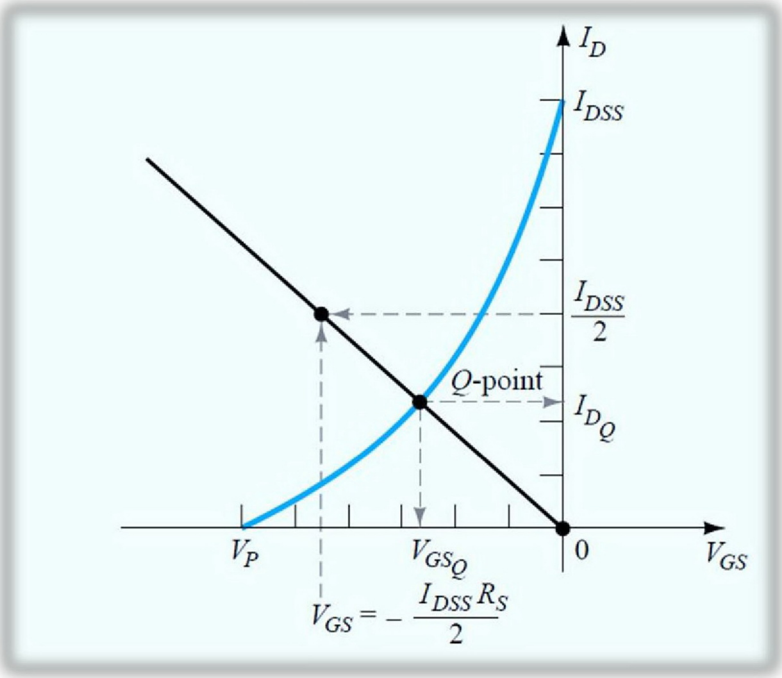
(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

SELF-BIAS CONFIGURATION

$$V_{GS} = -I_D R_S$$





$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

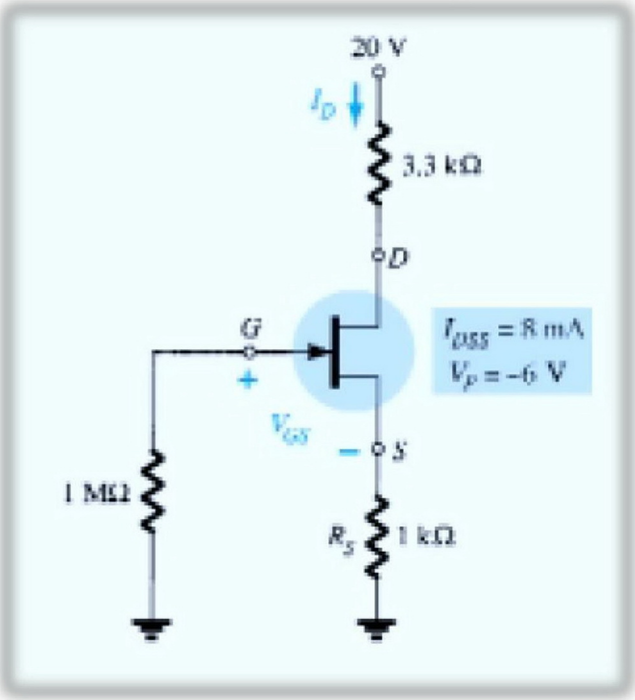
$$V_G = 0\ \text{V}$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

EXAMPLE

Determine the following for the network of Fig.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.



Solution

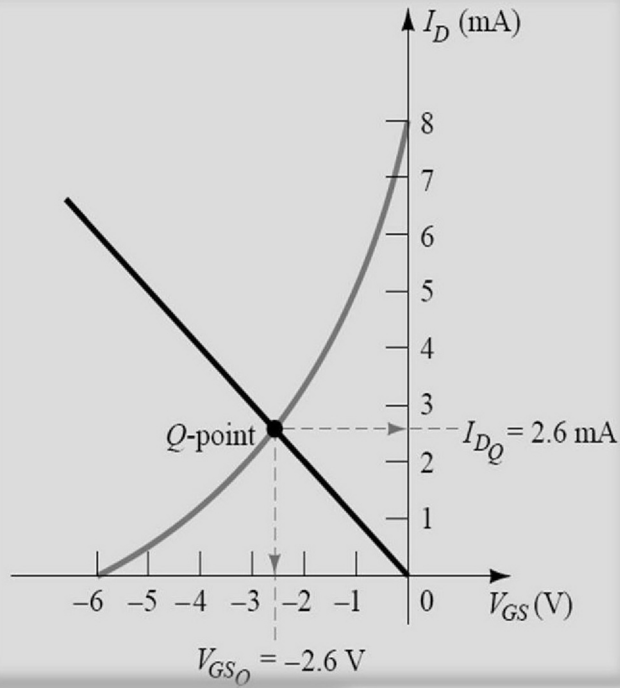
$$V_{GS} = -I_D R_S$$

$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

$$V_{GS_Q} = \mathbf{-2.6\ V}$$

(b) At the quiescent point:

$$I_{D_Q} = \mathbf{2.6\ mA}$$



(c)
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega) \\ &= 20\text{ V} - 11.18\text{ V} \\ &= \mathbf{8.82\ V} \end{aligned}$$

(d)
$$\begin{aligned} V_S &= I_D R_S \\ &= (2.6\text{ mA})(1\text{ k}\Omega) \\ &= \mathbf{2.6\ V} \end{aligned}$$

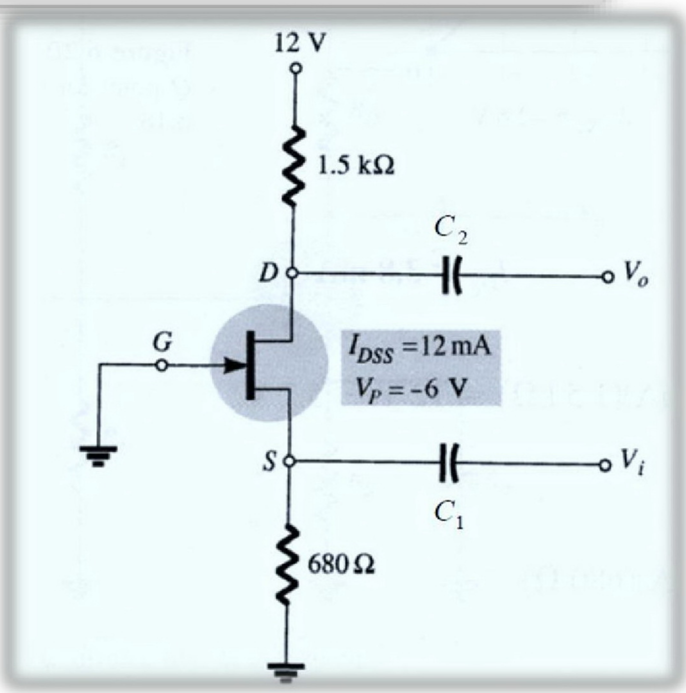
(e) $V_G = \mathbf{0\ V}$

(f) $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\ V}$

EXAMPLE

Determine the following for the common-gate configuration of Fig.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_D.
(d) V_G.
(e) V_S.
(f) V_{DS}.

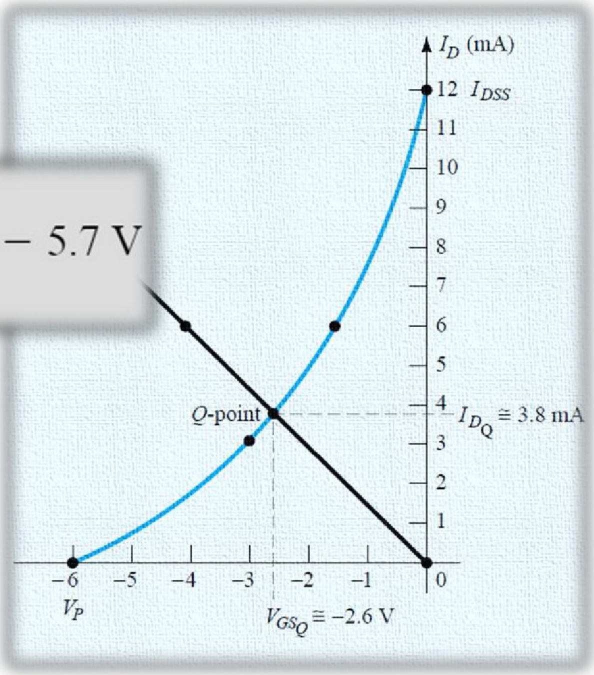


Solution

(a) $V_{GS_Q} \cong \mathbf{-2.6\ V}$

(b) $I_{D_Q} \cong \mathbf{3.8\ mA}$

(c) $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\ V}$



(d) $V_G = \mathbf{0\ V}$

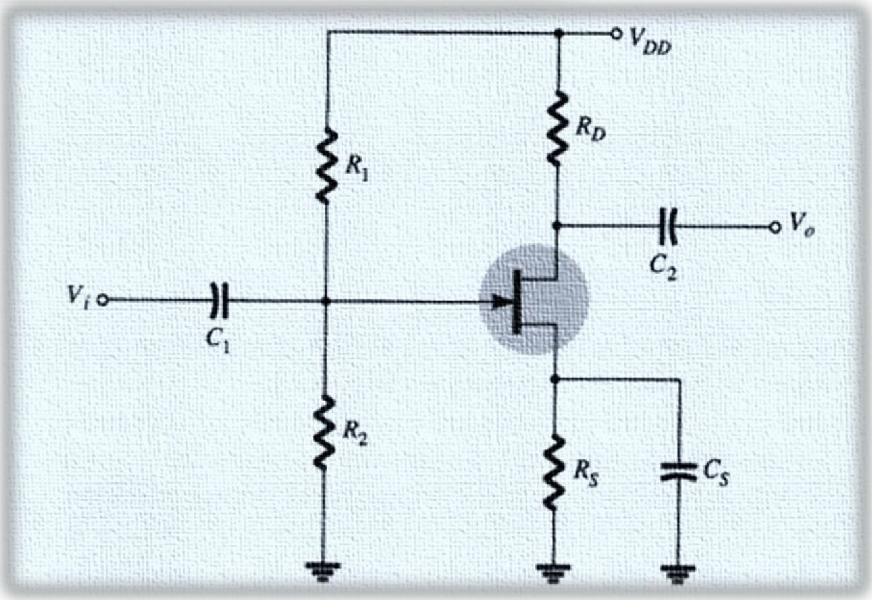
(e)

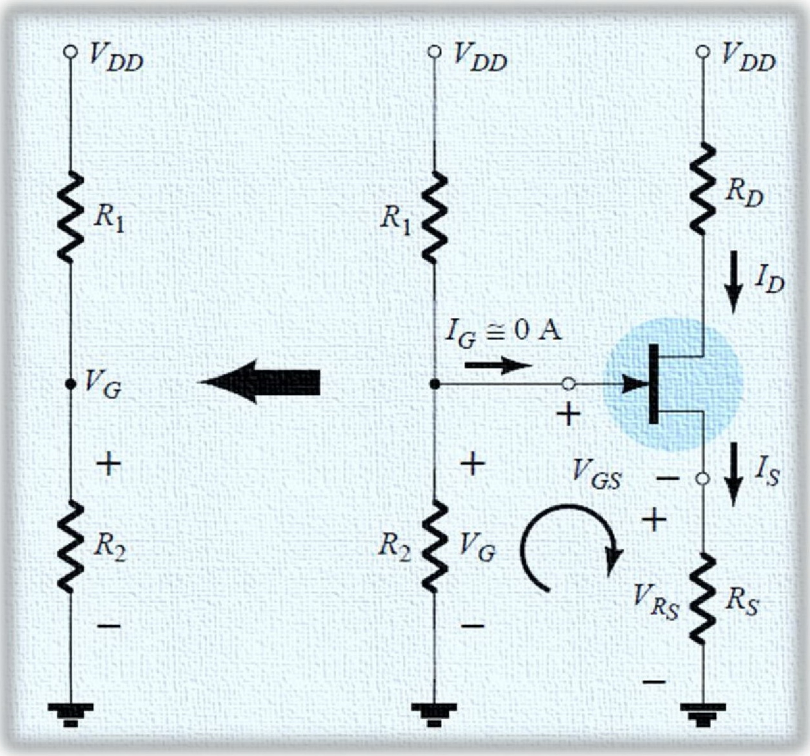
$$V_S = I_D R_S = (3.8 \text{ mA})(680\ \Omega)$$
$$= \mathbf{2.58\ V}$$

(f)

$$V_{DS} = V_D - V_S$$
$$= 6.3 \text{ V} - 2.58 \text{ V}$$
$$= \mathbf{3.72\ V}$$

VOLTAGE-DIVIDER BIASING





$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

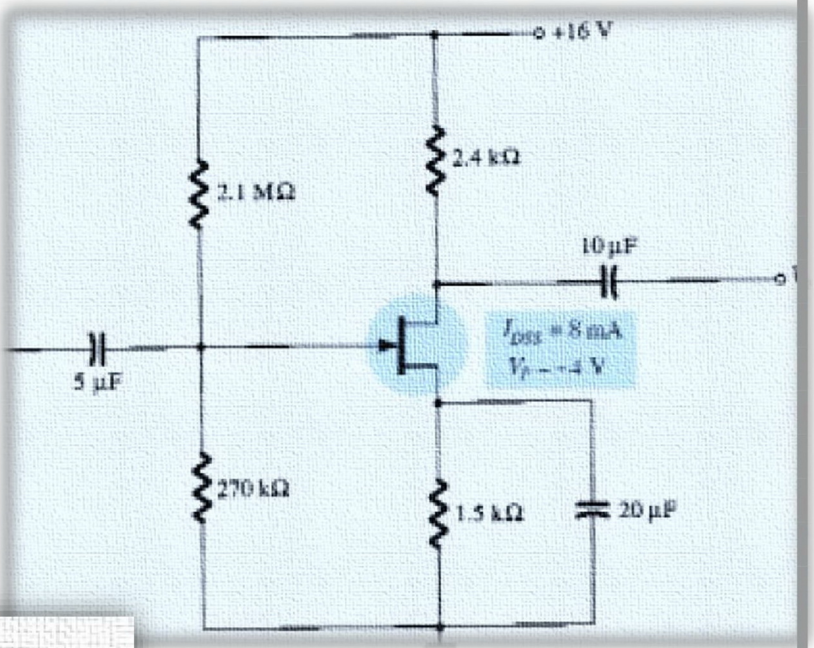
$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

EXAMPLE

Determine the following for the network of Fig.

(a) I_{D_Q} and V_{GS_Q}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.

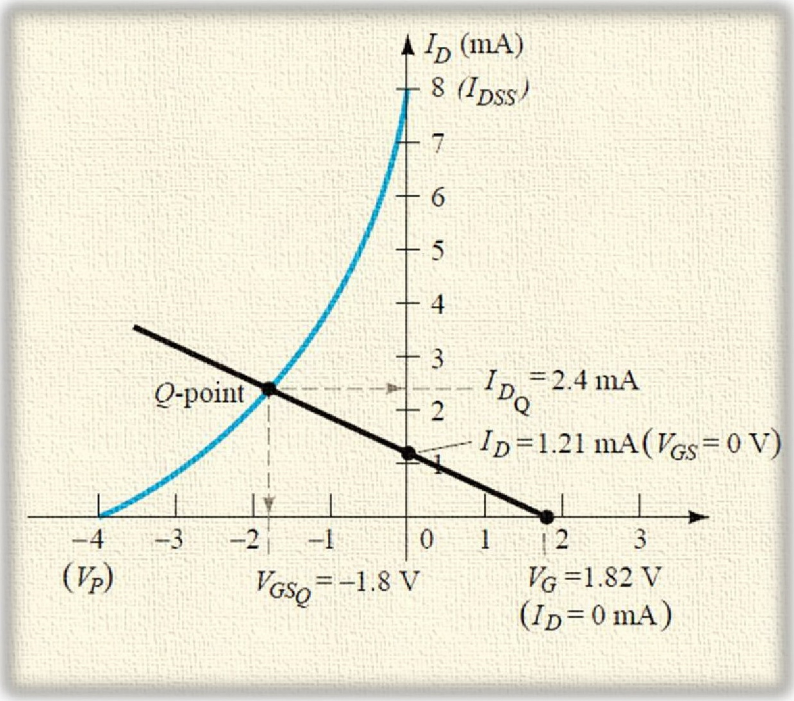


Solution

(a)
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$
$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$
$$= 1.82\ \text{V}$$

$$V_{GS} = V_G - I_D R_S$$
$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

$$I_{D_Q} = \mathbf{2.4\ mA}$$
$$V_{GS_Q} = \mathbf{-1.8\ V}$$



$$\begin{aligned}
\text{(b)}\ V_D &= V_{DD} - I_D R_D \\
&= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega) \\
&= \mathbf{10.24\ V}
\end{aligned}$$

$$\begin{aligned}
\text{(c)}\ V_S &= I_D R_S = (2.4\ \text{mA})(1.5\ \text{k}\Omega) \\
&= \mathbf{3.6\ V}
\end{aligned}$$

$$\begin{aligned}
\text{(d)}\ V_{DS} &= V_{DD} - I_D(R_D + R_S) \\
&= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega + 1.5\ \text{k}\Omega) \\
&= \mathbf{6.64\ V}
\end{aligned}$$

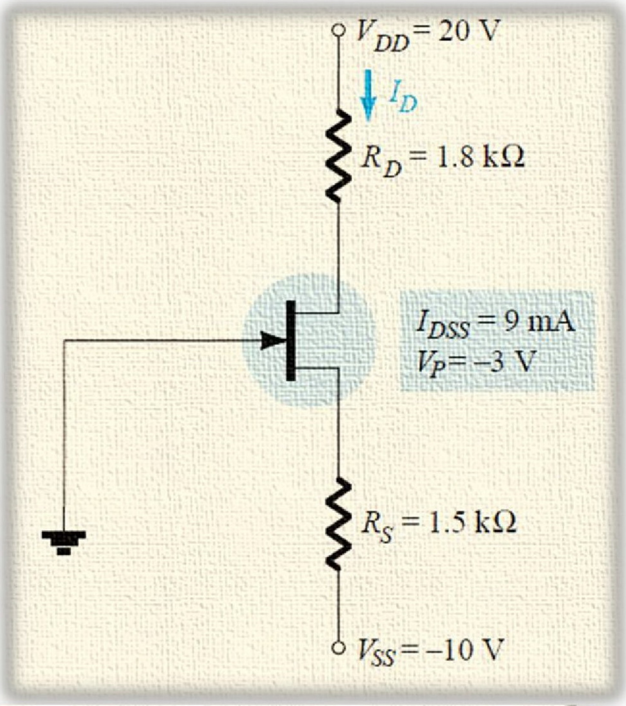
or $V_{DS} = V_D - V_S = 10.24\ \text{V} - 3.6\ \text{V}$
$= \mathbf{6.64\ V}$

(e) $V_{DG} = V_D - V_G$
$= 10.24\ \text{V} - 1.82\ \text{V}$
$= \mathbf{8.42\ V}$

EXAMPLE

Determine the following for the network of Fig.

(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.
(d) V_S.

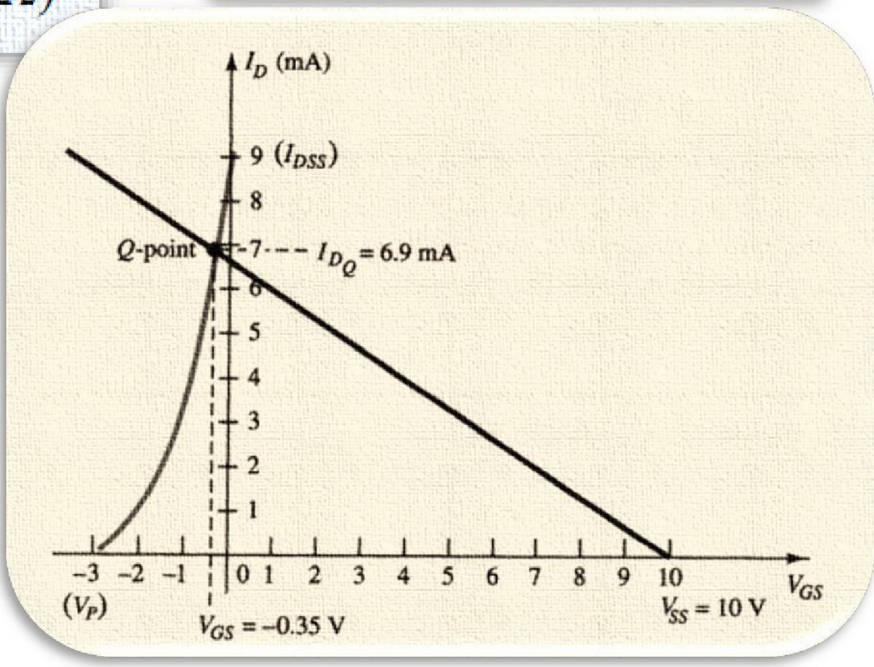


Solution

(a)

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

$$V_{GS} = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$



$$I_{D_Q} = \mathbf{6.9\ mA}$$

$$V_{GS_Q} = \mathbf{-0.35\ V}$$

(b) $$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)}$$

$$V_{DS} = 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= 30\text{ V} - 22.77\text{ V}$$
$$= \mathbf{7.23\text{ V}}$$

(c) $$V_D = V_{DD} - I_D R_D$$
$$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$$
$$= \mathbf{7.58\text{ V}}$$

(d) $$V_{DS} = V_D - V_S$$
or $$V_S = V_D - V_{DS}$$
$$= 7.58\text{ V} - 7.23\text{ V}$$
$$= \mathbf{0.35\text{ V}}$$

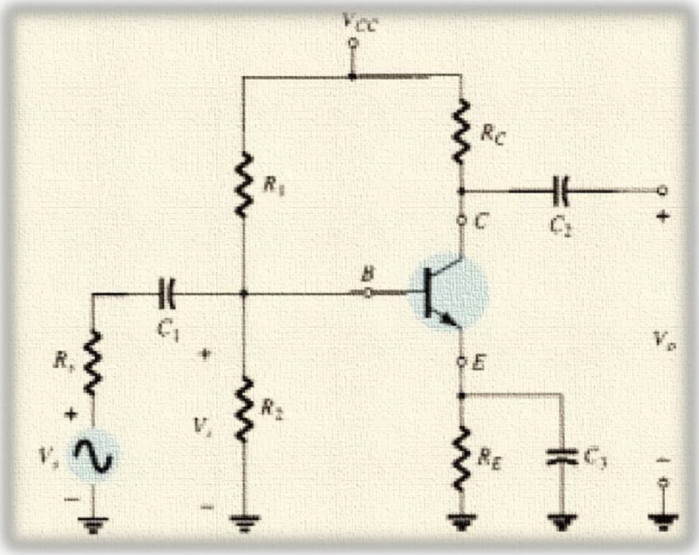
BJT Modeling and AC Equivalent Circuit

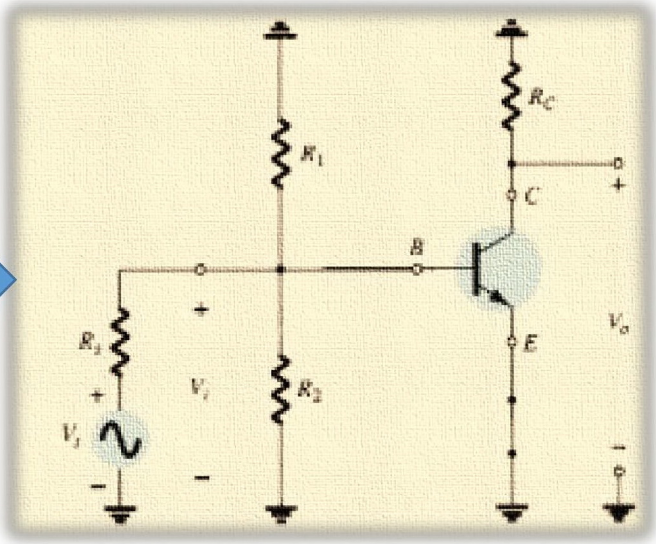
Basic Concepts:

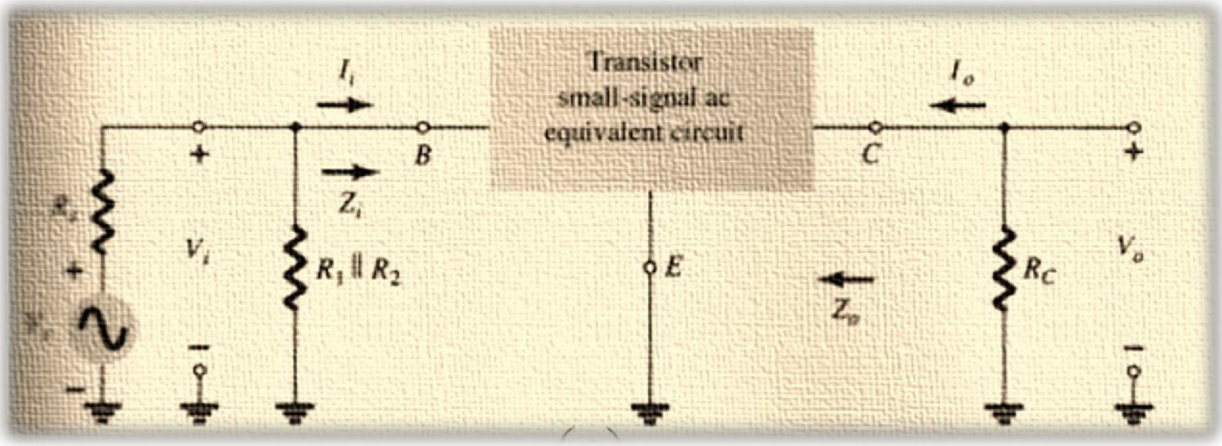
The key to the transistor small-signal analysis is the use of ac equivalent circuits or models. A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device (BJT) under specific operating conditions. Once the ac equivalent circuit has been determined, the graphical symbol of the device can be replaced in the schematic by this circuit and the basic methods of ac circuit analysis (mesh analysis, nodal analysis, and Thevenin's theorem) can be applied to determine the response of the circuit. There are two schools of thought in prominence today regarding the equivalent circuit to be substituted for the transistor: ***hybrid*** and ***r_e model***.

In summary, the ac equivalent circuit of the BJT amplifier is obtained by

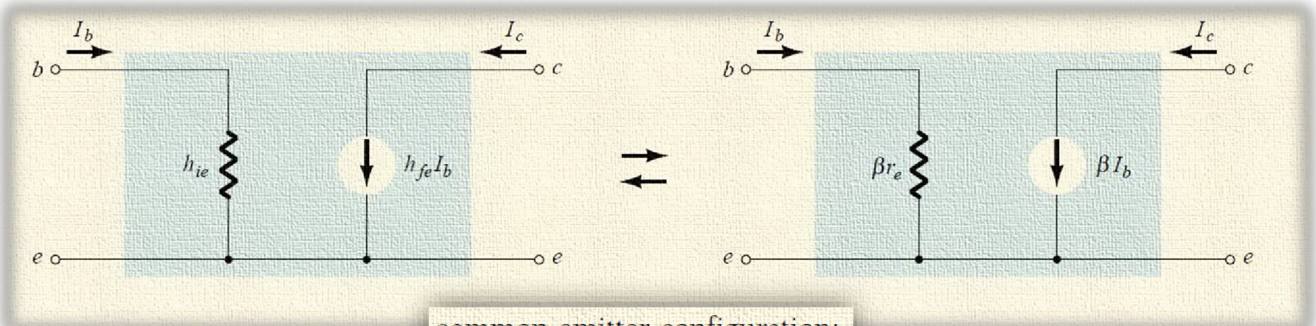
1. Setting all dc sources to zero and replacing them by a short-circuit equivalent.
2. Replacing all capacitors by a short-circuit equivalent.
3. Removing all elements bypassed by the short-circuit equivalents introduced by stapes 1 and 2.
4. Redrawing the circuit in a more convenient and logical form.
5. Use the ***hybrid*** or ***r_e*** equivalent circuit of the BJT to complete the equivalent circuit of the amplifier.
6. Finally, the following parameters are determined for the amplifier:
   a. Input impedance (Z_i). b. Output impedance (Z_o). c. Voltage gain (A_v).
   d. Current gain (A_i). e. Phase relationship (θ).


V_{CC}
R_C
R_1
C_2
C
B
C_1
R_s
E
V_o
R_2
V_i
V_s
R_E
C_3

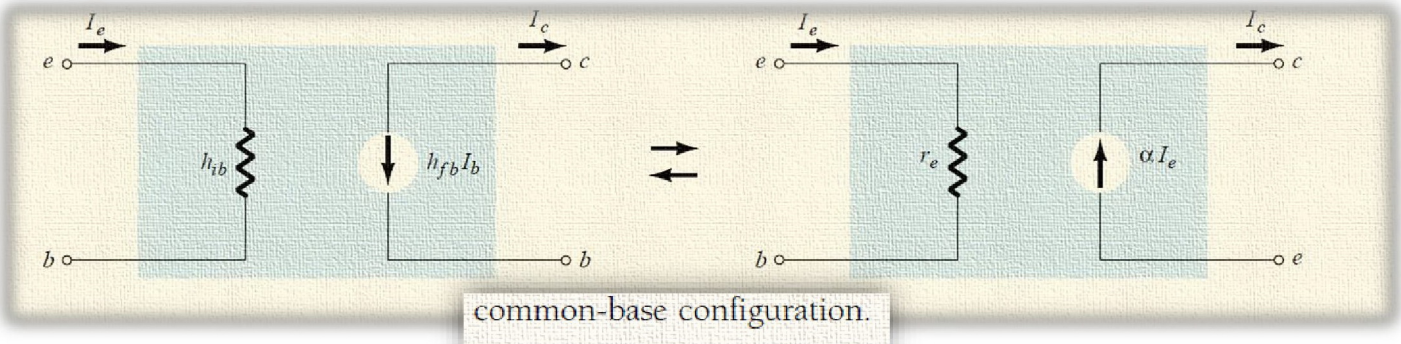

R_C
R_1
C
B
R_s
V_i
R_2
E
V_o
V_s


Transistor
small-signal ac
equivalent circuit
I_i
I_o
B
C
Z_i
V_i
$R_1 \parallel R_2$
E
Z_o
R_C
V_o

Hybrid versus r_e model:



common-emitter configuration;



common-base configuration.

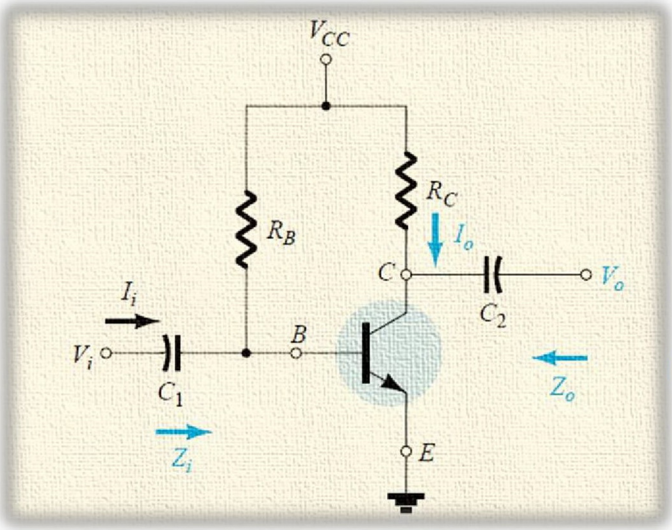
$$\boxed{h_{ie} = \beta r_e}$$

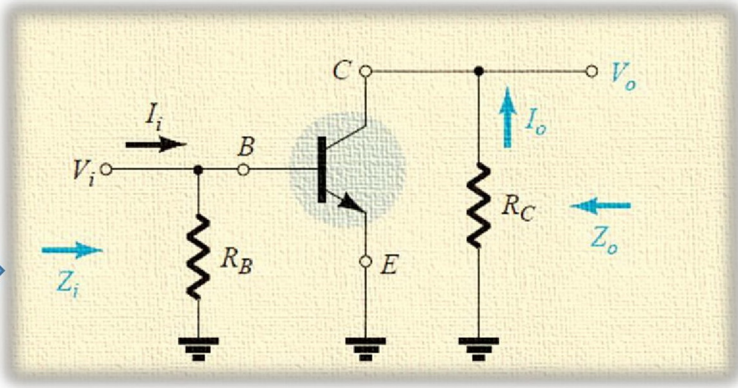
$$\boxed{h_{fe} = \beta_{ac}}$$

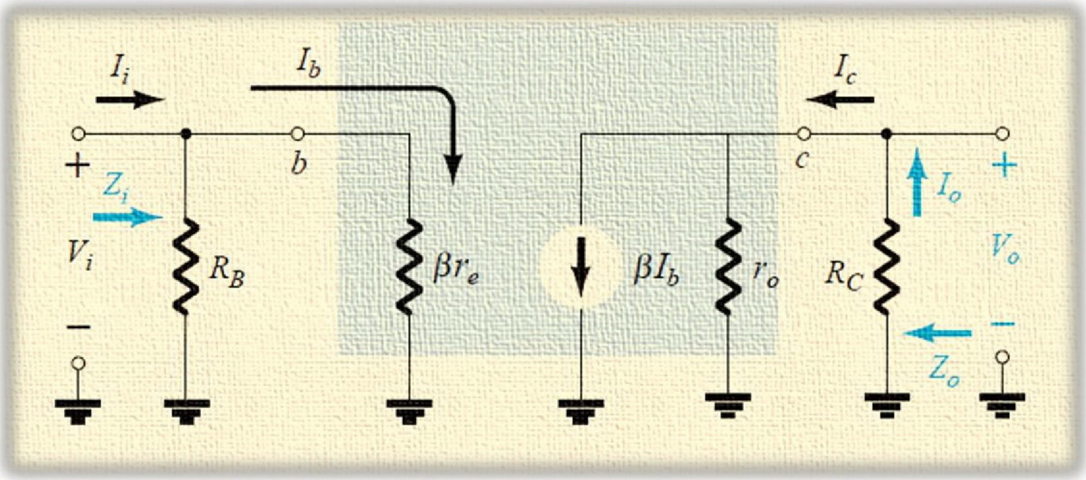
$$\boxed{h_{fb} = -\alpha \cong -1}$$

$$\boxed{h_{ib} = r_e}$$

COMMON-EMITTER FIXED-BIAS CONFIGURATION







$$\boxed{Z_i = R_B \| \beta r_e}$$

$$\boxed{Z_i \cong \beta r_e}_{R_B \geq 10\beta r_e} \quad \text{ohms}$$

$$\boxed{Z_o = R_C \| r_o} \quad \text{ohms}$$

$$\boxed{Z_o \cong R_C}_{r_o \geq 10 R_C}$$

$$V_o = -\beta I_b (R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta_{re}}\right)(R_C \| r_o)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}}$$

If $r_o \geq 10R_C$,

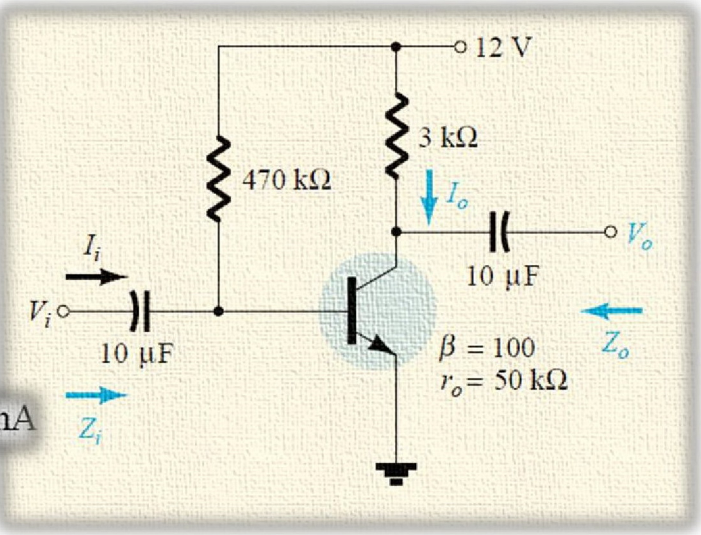
$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10R_C}$$

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}}$$

$$\boxed{A_i \cong \beta}_{r_o \geq 10R_C,\ R_B \geq 10\beta r_e}$$

EXAMPLE

For the network of Fig.
(a) Determine r_e.
(b) Find Z_i (with $r_o = \infty\ \Omega$).
(c) Calculate Z_o (with $r_o = \infty\ \Omega$).
(d) Determine A_v (with $r_o = \infty\ \Omega$).
(e) Find A_i (with $r_o = \infty\ \Omega$).
(f) Repeat parts (c) through (e) including $r_o = 50\ \text{k}\Omega$ in all calculations and compare results.



Solution

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.069\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

$$\text{(d)}\ A_v = -\frac{R_C}{r_e} = -\frac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

(e) Since $R_B \geq 10\beta r_e (470\ \text{k}\Omega > 10.71\ \text{k}\Omega)$

$A_i \cong \beta = \mathbf{100}$

(f) $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}$ vs. $3\ \text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24} \text{ vs. } -280.11$$

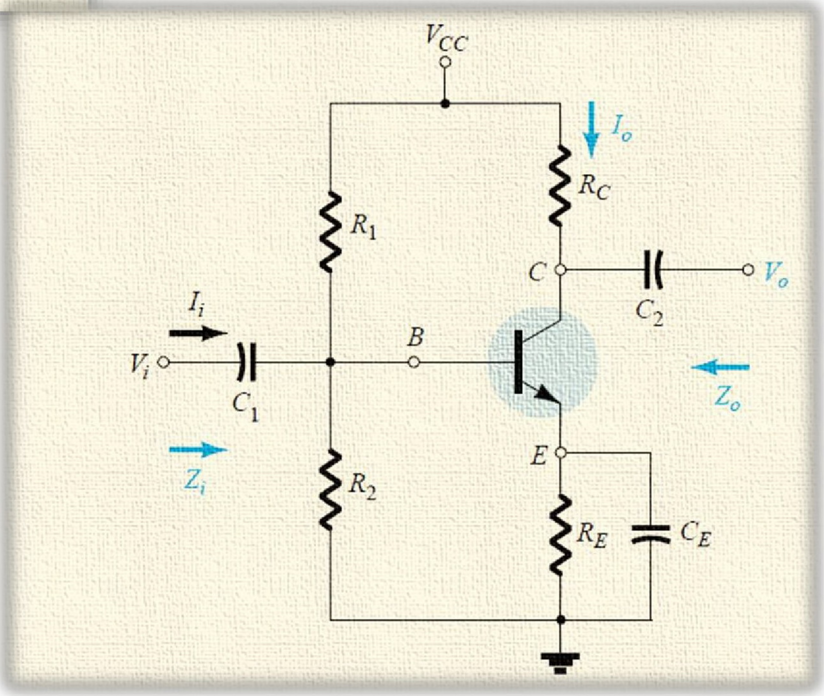
$$A_i = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 3\ \text{k}\Omega)(470\ \text{k}\Omega + 1.071\ \text{k}\Omega)}$$

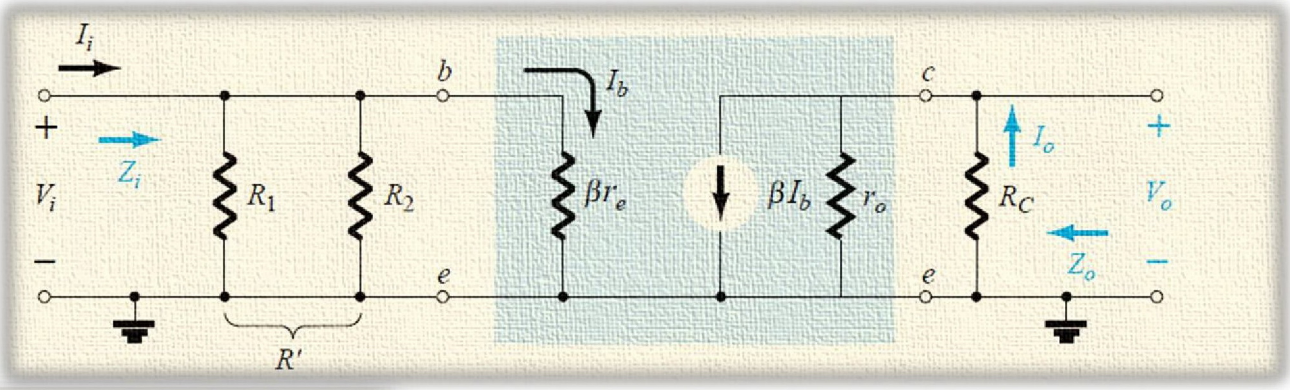
$$= \mathbf{94.13} \text{ vs. } 100$$

As a check:

$$A_i = -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ \text{k}\Omega)}{3\ \text{k}\Omega} = \mathbf{94.16}$$

VOLTAGE-DIVIDER BIAS





$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \| \beta r_e$$

$$\boxed{Z_o = R_C \| r_o}$$

$$\boxed{Z_o \cong R_C}_{\,r_o \geq 10 R_C}$$

$$V_o = -(\beta I_b)(R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

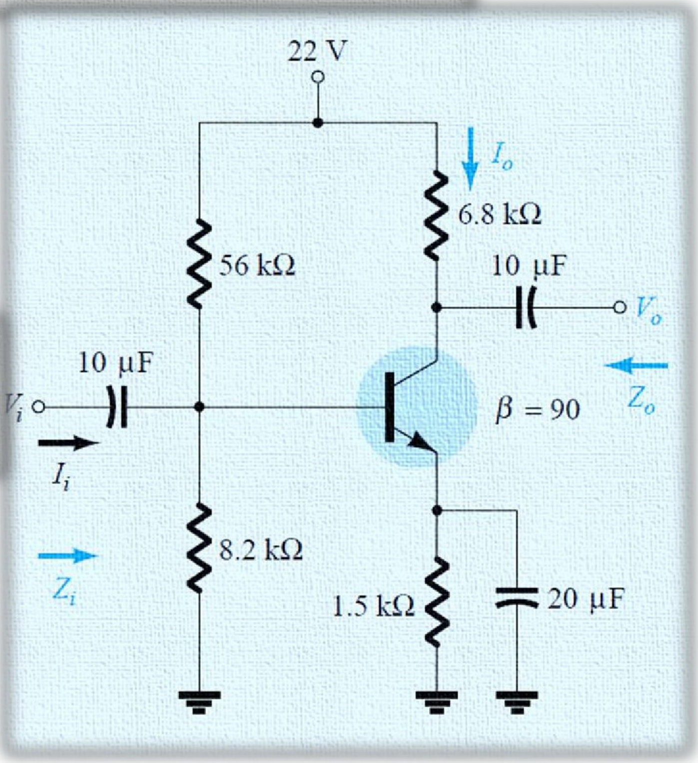
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}}$$

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}}$$

EXAMPLE

For the network of Fig. , determine:

(a) r_e.
(b) Z_i.
(c) Z_o ($r_o = \infty\ \Omega$).
(d) A_v ($r_o = \infty\ \Omega$).
(e) A_i ($r_o = \infty\ \Omega$).
(f) The parameters of parts (b) through (e) if $r_o = 1/h_{oe} = 50\ \text{k}\Omega$ and compare results.



Solution

(a)

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

(b) $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega = \mathbf{1.35\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{6.8\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

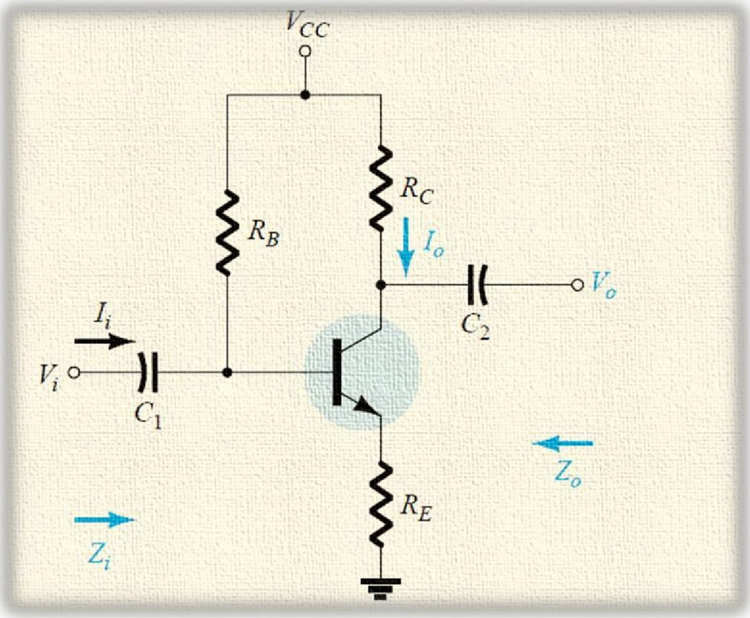
(e) $A_i =$? H.W

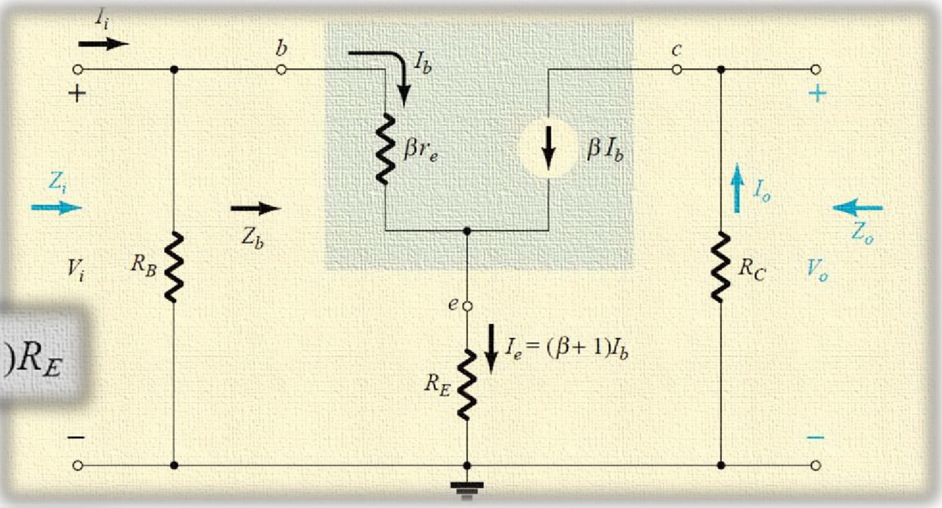
(f) $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. $6.8\ \text{k}\Omega$

$A_v = -\dfrac{R_C \| r_o}{r_e} = -\dfrac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. -368.76

CE EMITTER-BIAS CONFIGURATION





$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E}$$

$$\boxed{Z_b \cong \beta(r_e + R_E)}$$

$$\boxed{Z_i = R_B \| Z_b}$$

$$\boxed{Z_o = R_C}$$

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o\, R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right) R_C$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}}$$

Substituting $Z_b = \beta(r_e + R_E)$ gives

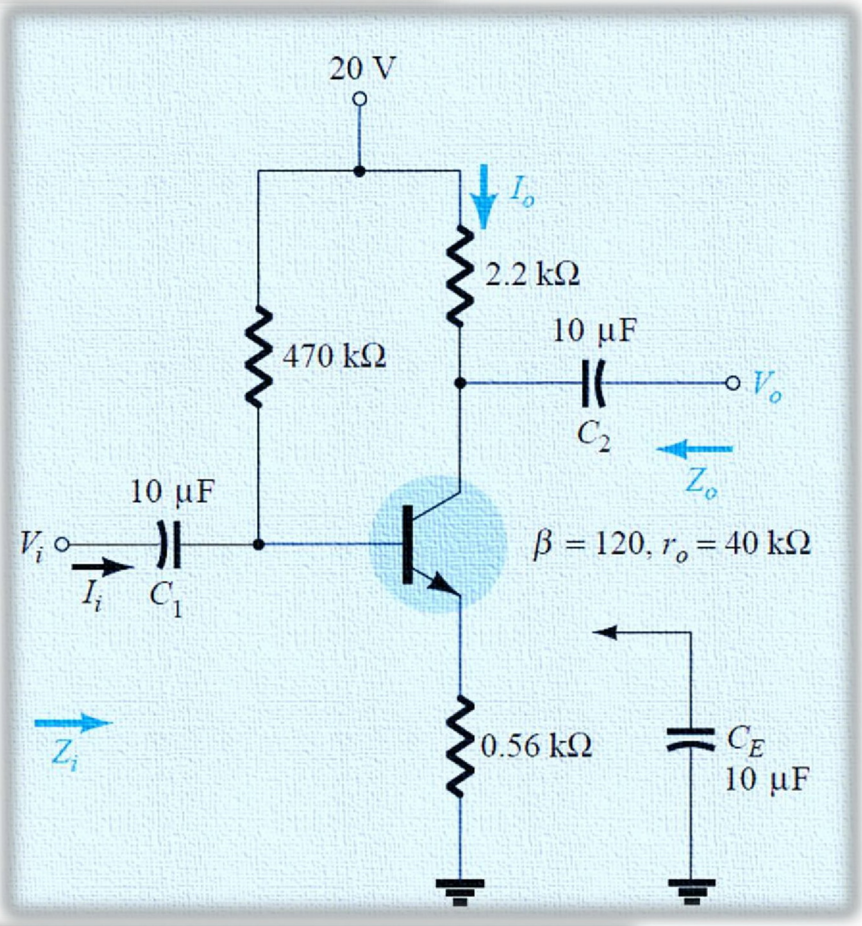
$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}}$$

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}}$$

EXAMPLE

For the network of Fig. without C_E (unbypassed), determine:

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.



Solution

(a) DC: $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \dfrac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$

$$I_E = (\beta + 1)I_B = (121)(46.5\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

(b) $Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$

$= 67.92\ \text{k}\Omega$

$Z_i = R_B \| Z_b = 470\ \text{k}\Omega \| 67.92\ \text{k}\Omega$

$= \mathbf{59.34\ k\Omega}$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\ \text{k}\Omega)}{67.92\ \text{k}\Omega}$$

$= \mathbf{-3.89}$

(e) $$A_i = -A_v \frac{Z_i}{R_C} = -(-3.89)\left(\frac{59.34\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$$

$= \mathbf{104.92}$

Exercises

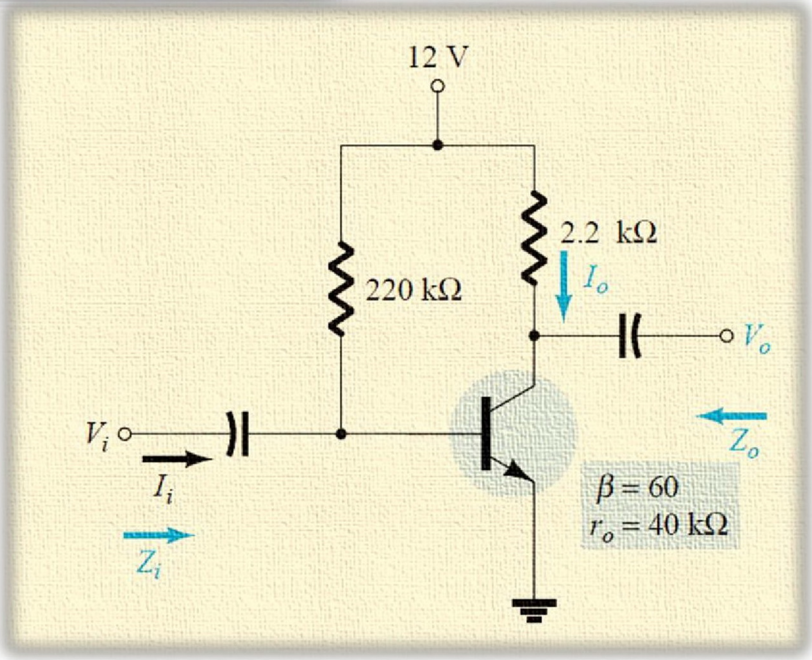
1. For the network of Fig.

(a) Determine Z_i and Z_o.

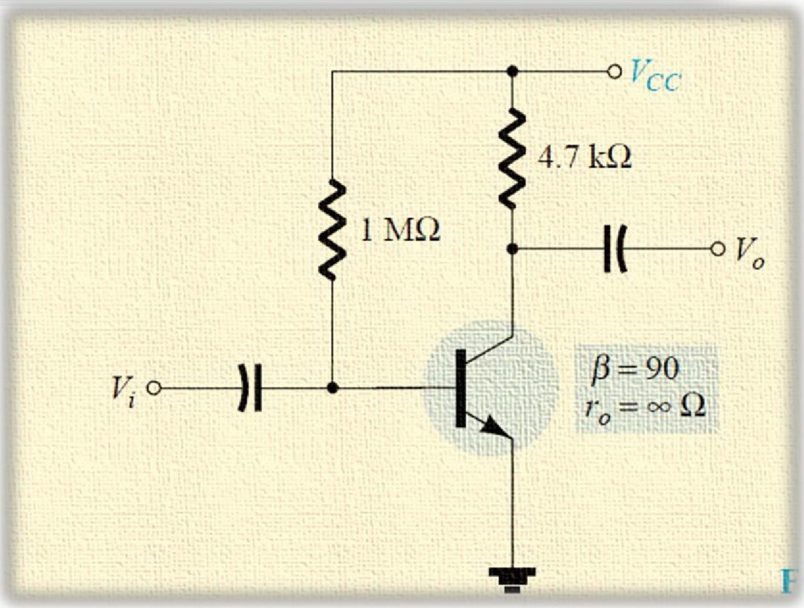
(b) Find A_v and A_i.

(c) Repeat part (a) with $r_o = 20\ \text{k}\Omega$.

(d) Repeat part (b) with $r_o = 20\ \text{k}\Omega$.



2. For the network of Fig. , determine V_{CC} for a voltage gain of $A_v = -200$.



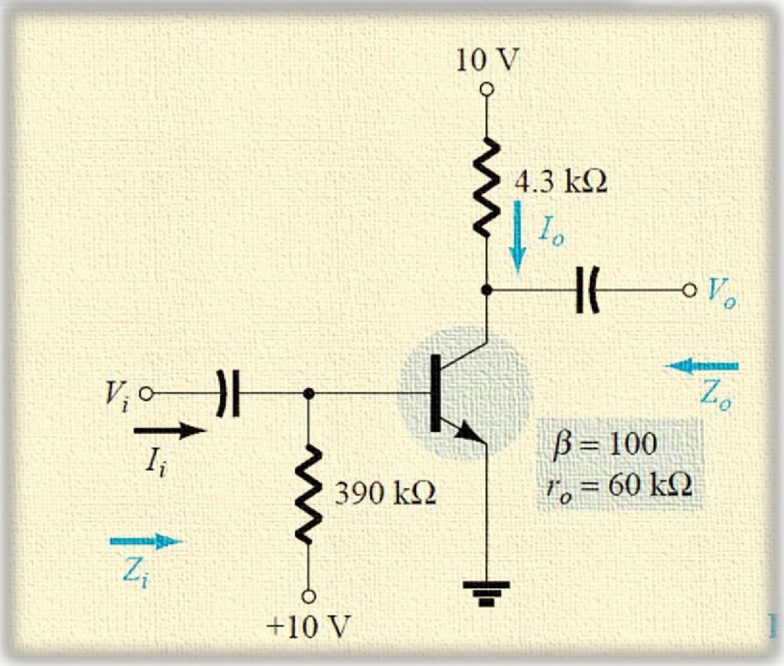
* **3.** For the network of Fig.

(a) Calculate I_B, I_C, and r_e.

(b) Determine Z_i and Z_o.

(c) Calculate A_v and A_i.

(d) Determine the effect of $r_o = 30\ \text{k}\Omega$ on A_v and A_i.



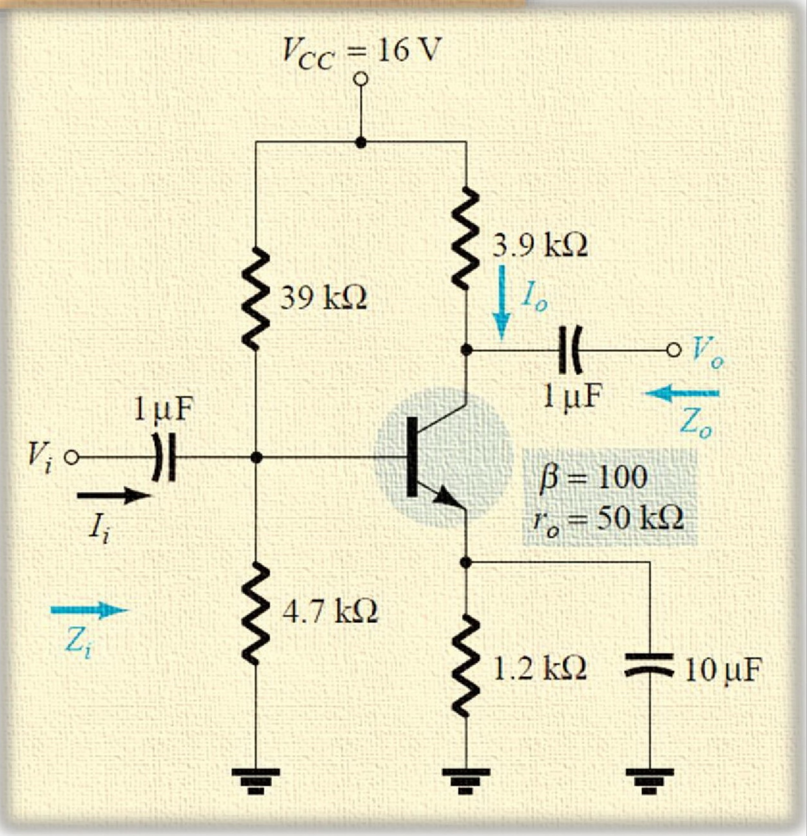
4. For the network of Fig.

(a) Determine r_e.

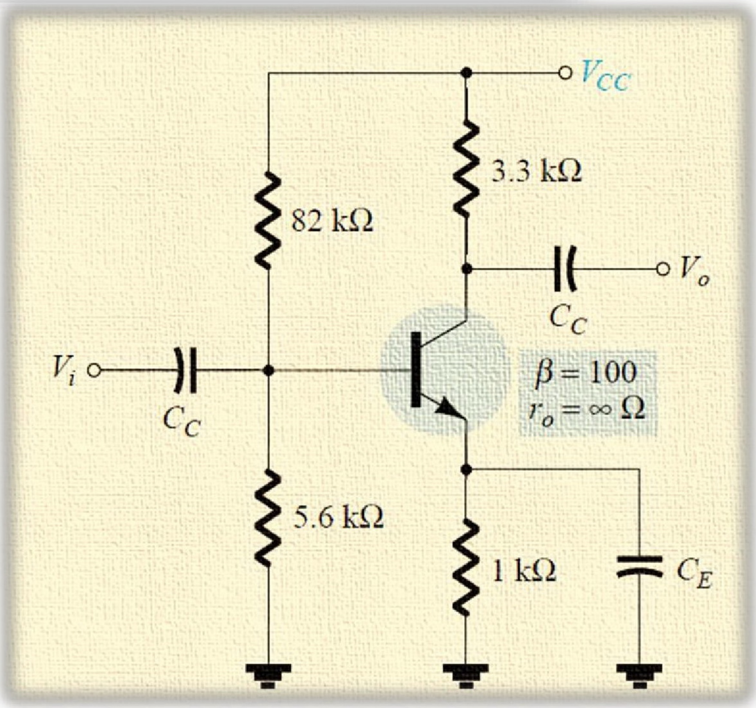
(b) Calculate Z_i and Z_o.

(c) Find A_v and A_i.

(d) Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.



5. Determine V_{CC} for the network of Fig. if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.



JFET Small-Signal Analysis

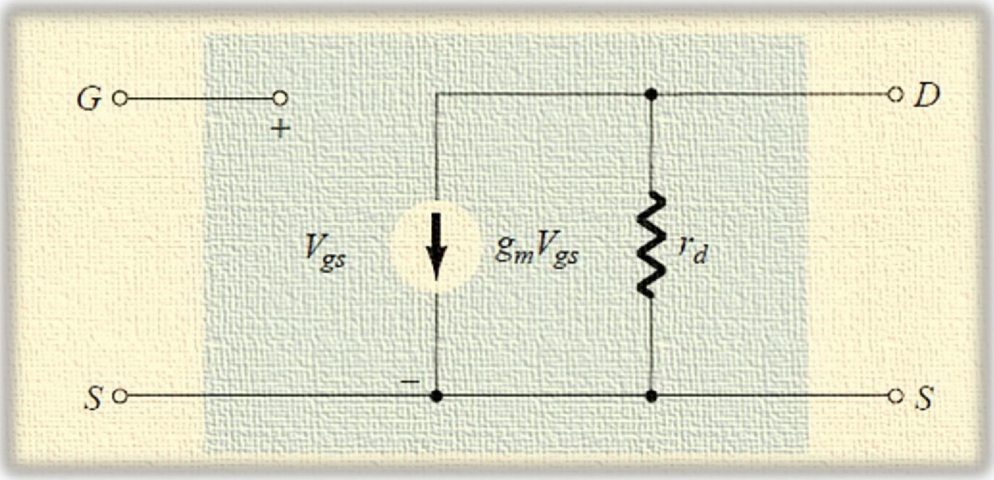
The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

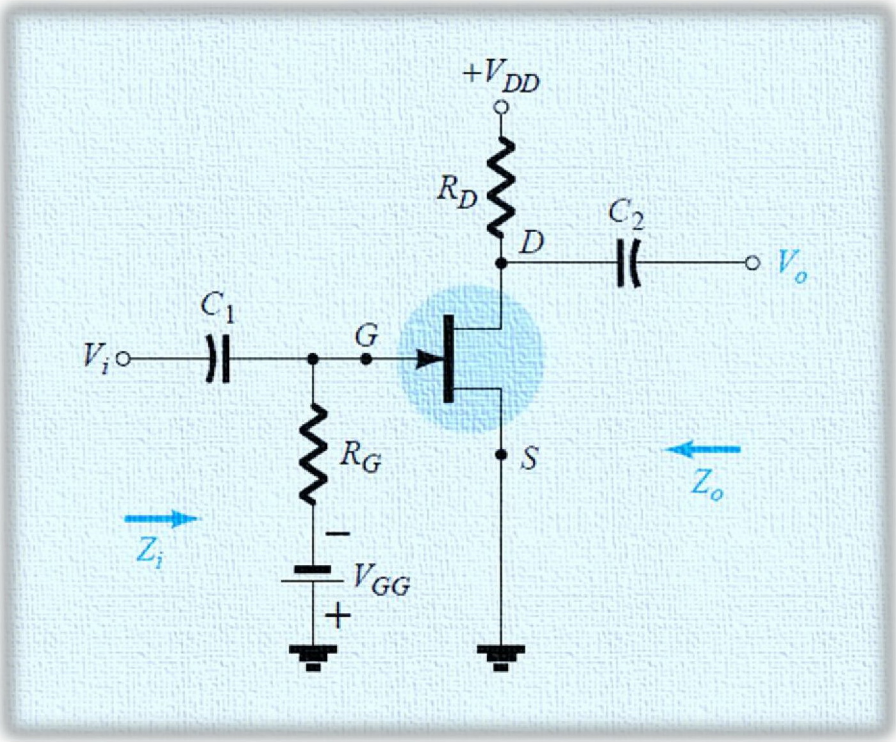
$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

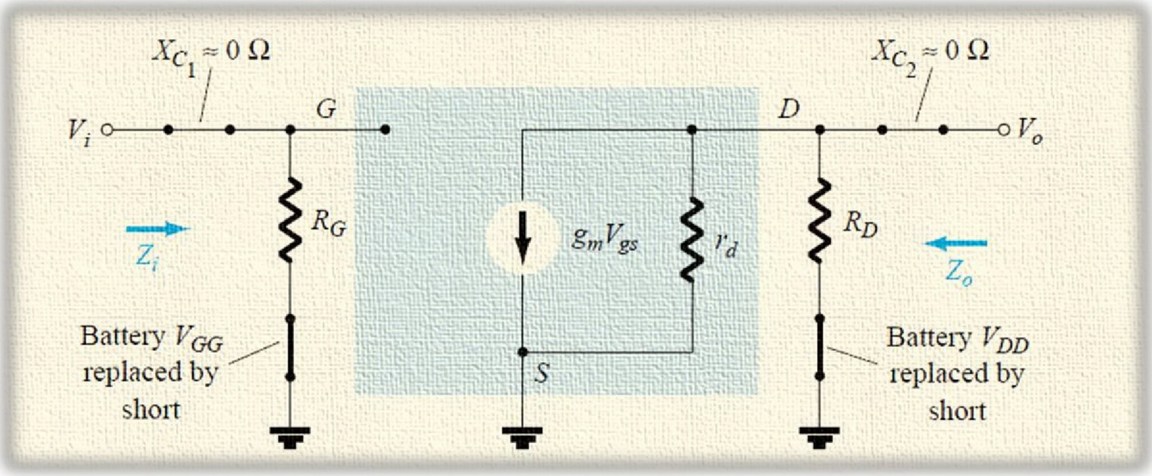
$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

FET AC Equivalent Circuit

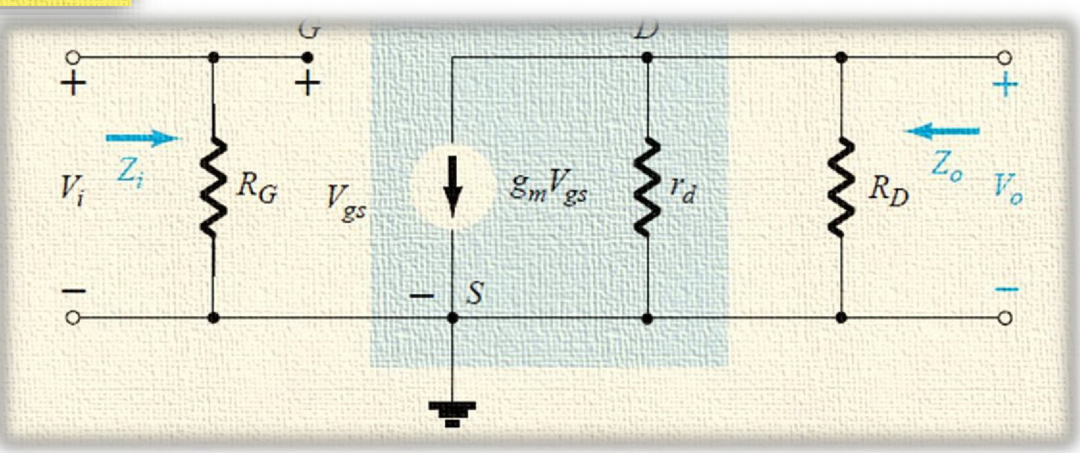


JFET FIXED-BIAS CONFIGURATION



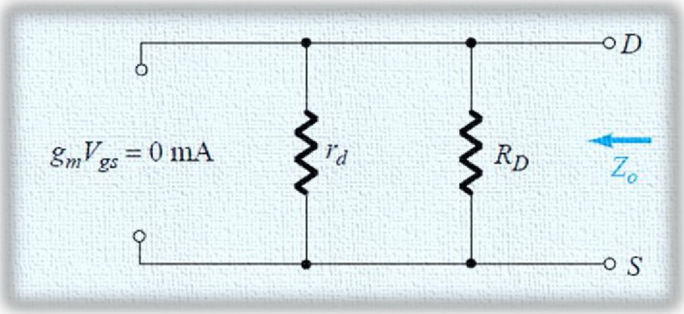


$$\boxed{Z_i = R_G}$$



$$\boxed{Z_o = R_D \| r_d}$$

$$\boxed{Z_o \cong R_D} \quad {}_{r_d \geq 10R_D}$$



$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_i(r_d \| R_D)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

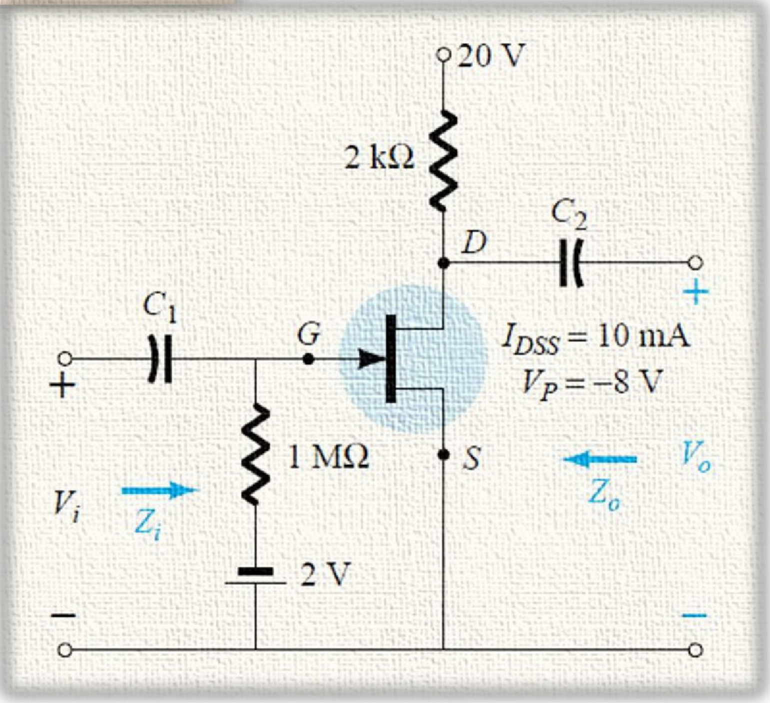
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D} \quad {}_{r_d \geq 10R_D}$$

EXAMPLE

The fixed-bias configuration

(a) Determine g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o.
(e) Determine the voltage gain A_v.
(f) Determine A_v ignoring the effects of r_d.

Solution



(a) $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{8 \text{ V}} = 2.5 \text{ mS}$

$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5 \text{ mS}\left(1 - \frac{(-2 \text{ V})}{(-8 \text{ V})}\right) = \mathbf{1.88 \text{ mS}}$

(b) $r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

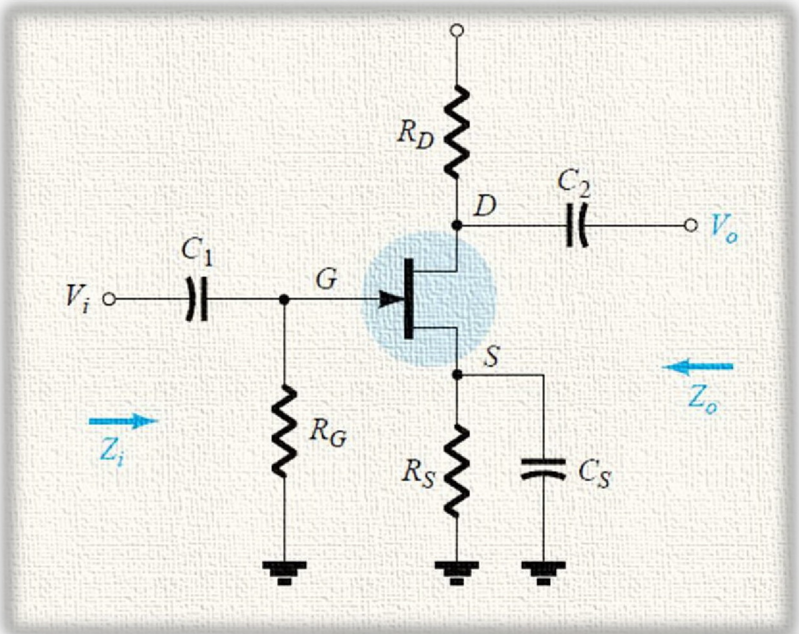
(d) $Z_o = R_D \| r_d = 2\ \text{k}\Omega \| 25\ \text{k}\Omega = \mathbf{1.85\ k\Omega}$

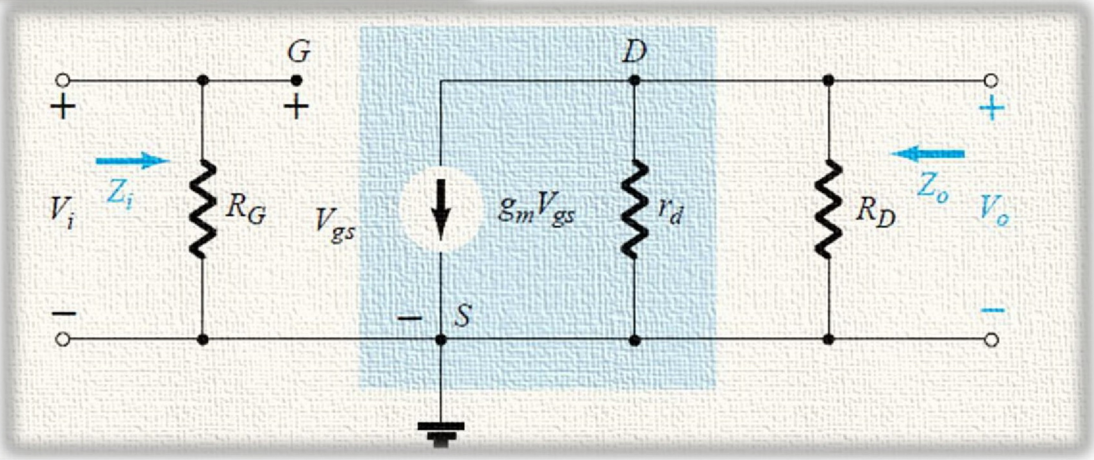
(e) $A_v = -g_m(R_D \| r_d) = -(1.88 \text{ mS})(1.85\ \text{k}\Omega)$

$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88 \text{ mS})(2\ \text{k}\Omega) = \mathbf{-3.76}$

JFET SELF-BIAS CONFIGURATION





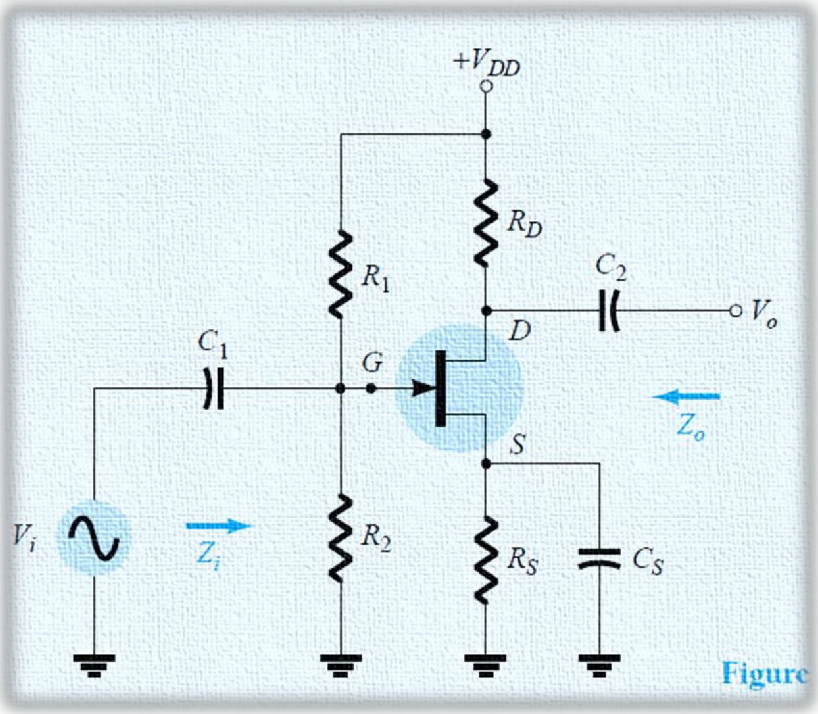
$$Z_i = R_G$$

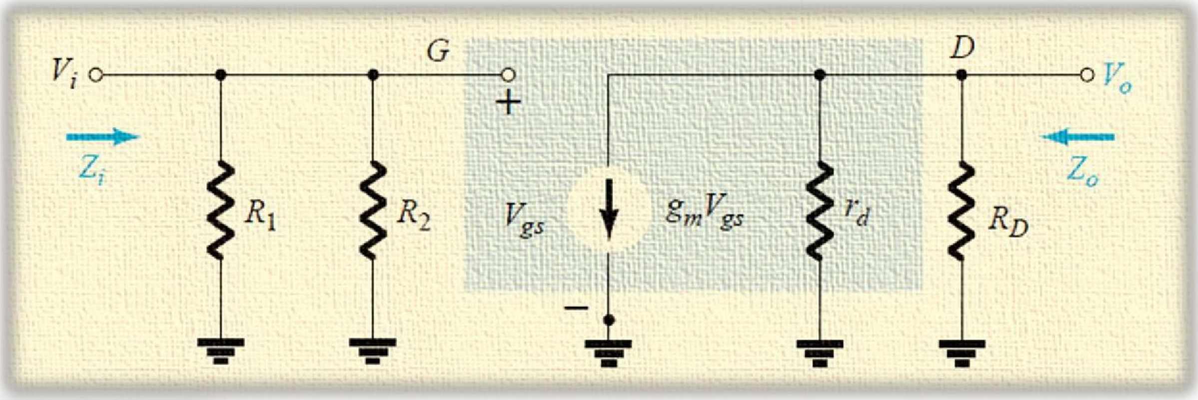
$$Z_o = r_d \| R_D$$

$$\boxed{A_v = -g_m(r_d \| R_D)}$$

$$\boxed{A_v = -g_m R_D}_{r_d \geq 10R_D}$$

JFET VOLTAGE-DIVIDER CONFIGURATION





$$\boxed{Z_i = R_1 \| R_2}$$

$$\boxed{Z_o = r_d \| R_D}$$

$$\boxed{Z_o \cong R_D}_{\, r_d \geq 10R_D}$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

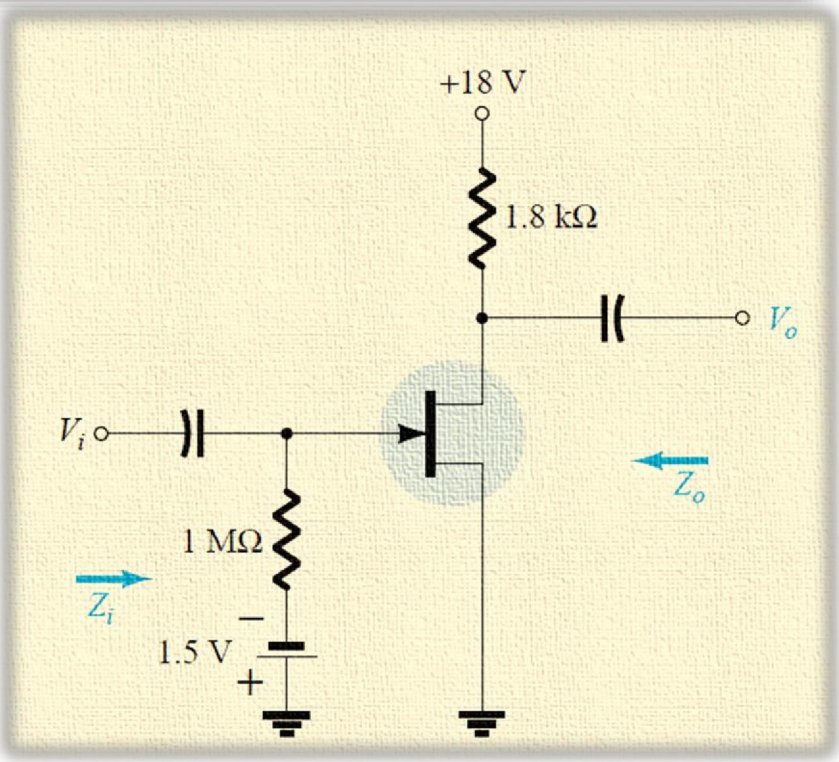
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}$$

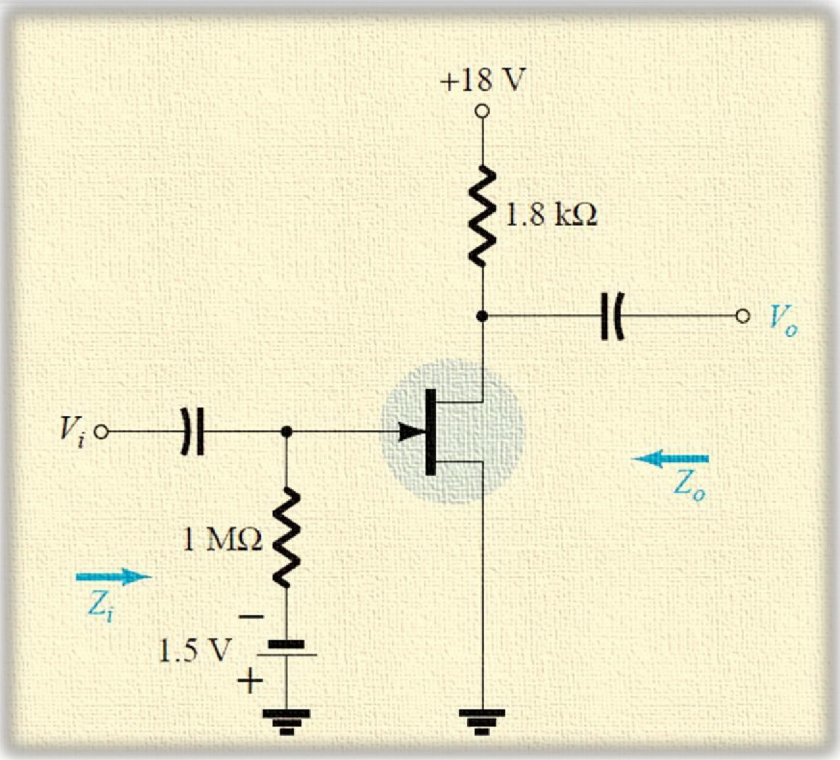
$r_d \geq 10R_D$

Exercises

1. Determine Z_i, Z_o and A_v for the network of Fig. if $I_{DSS} = 10$ mA, $V_P = -4$ V, and $r_d = 40$ kΩ.



2.Determine Z_i, Z_o, and A_v for the network of Fig. if $I_{DSS} = 12$ mA, $V_P = -6$ V, and $y_{os} = 40\ \mu$S.



3.Determine Z_i, Z_o, and A_v for the network of Fig. if $I_{DSS} = 6$ mA, $V_P = -6$ V, and $y_{os} = 40\ \mu$S.